

FIG.1

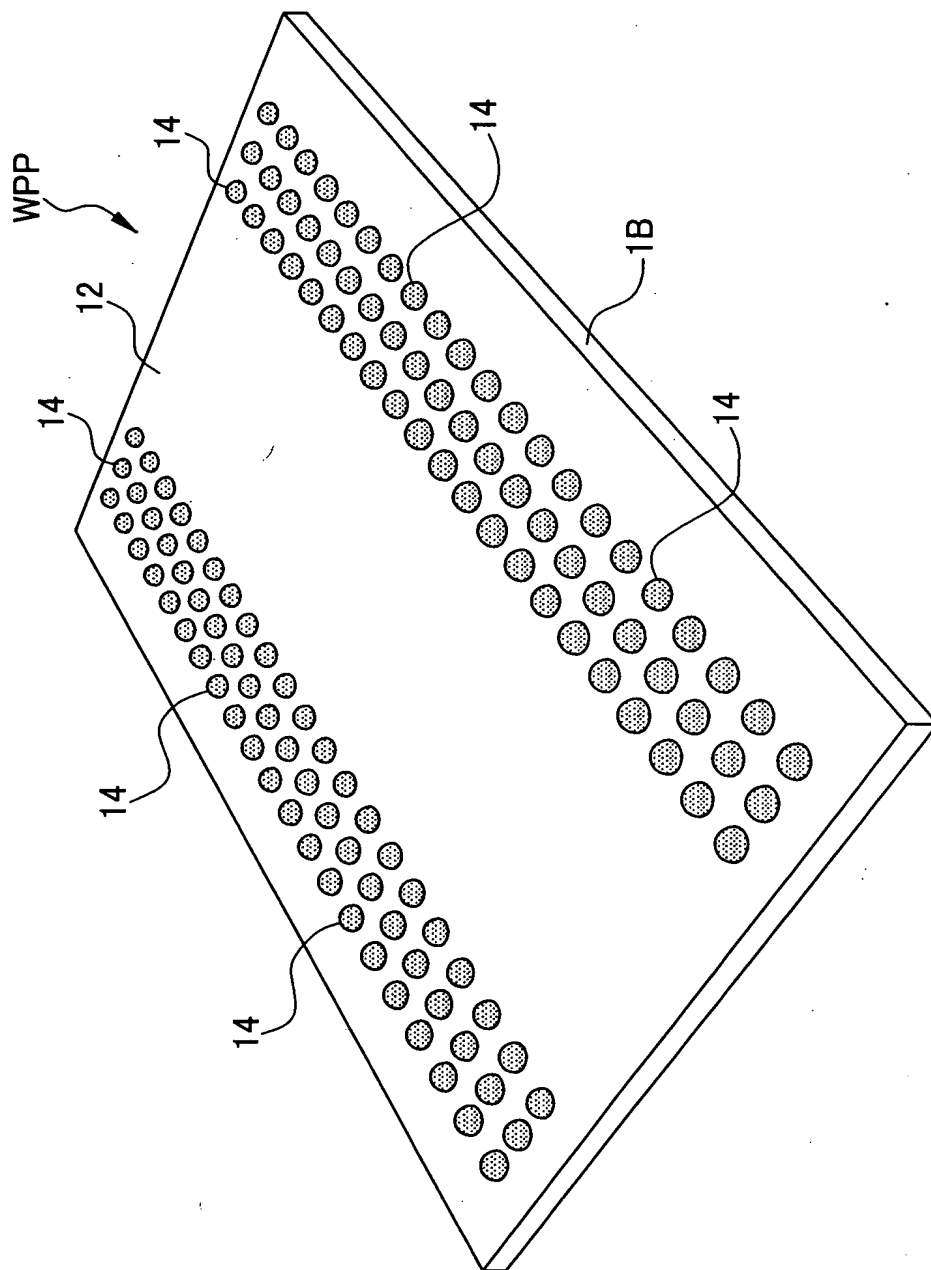


FIG.2

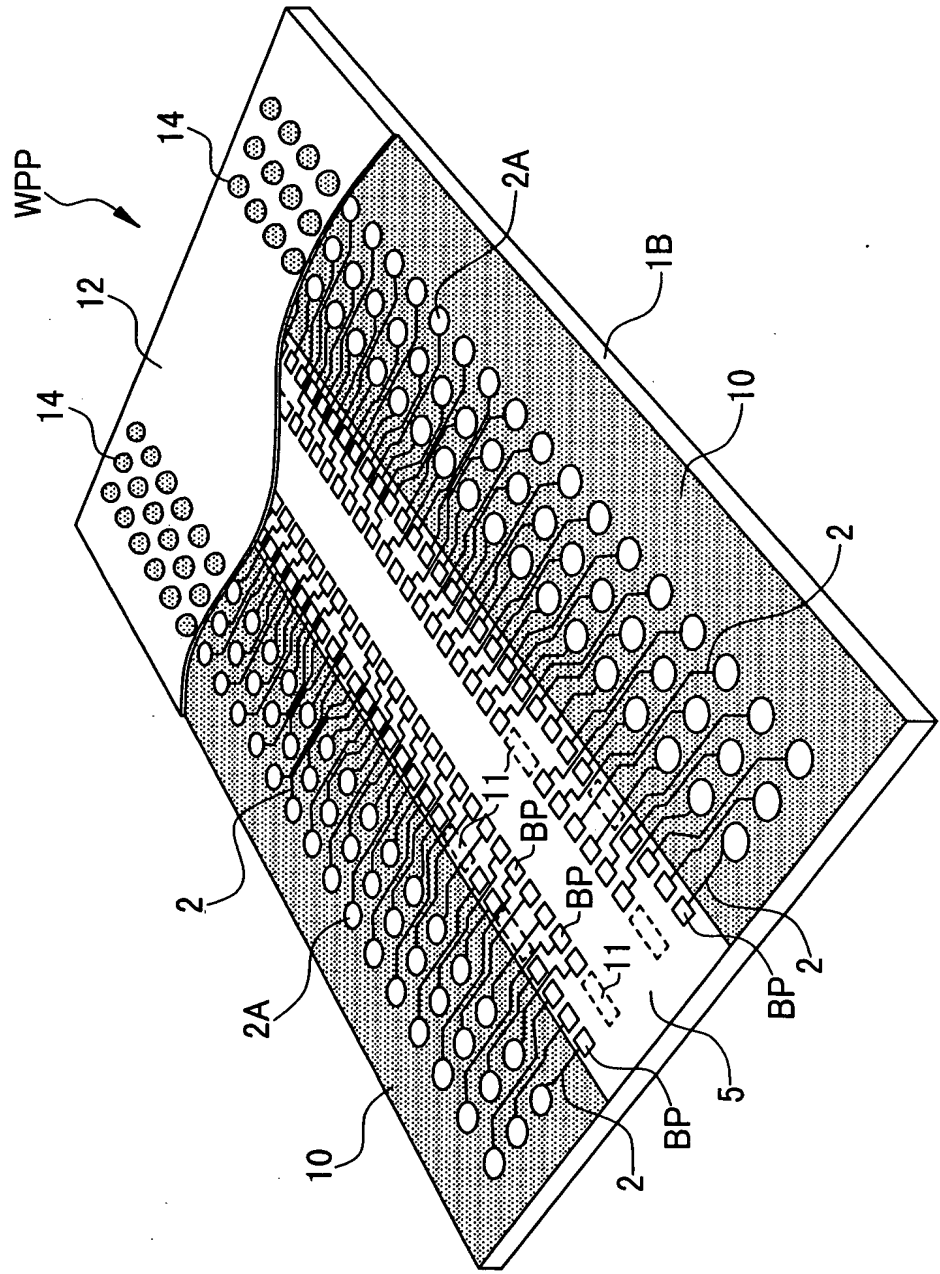


FIG.3

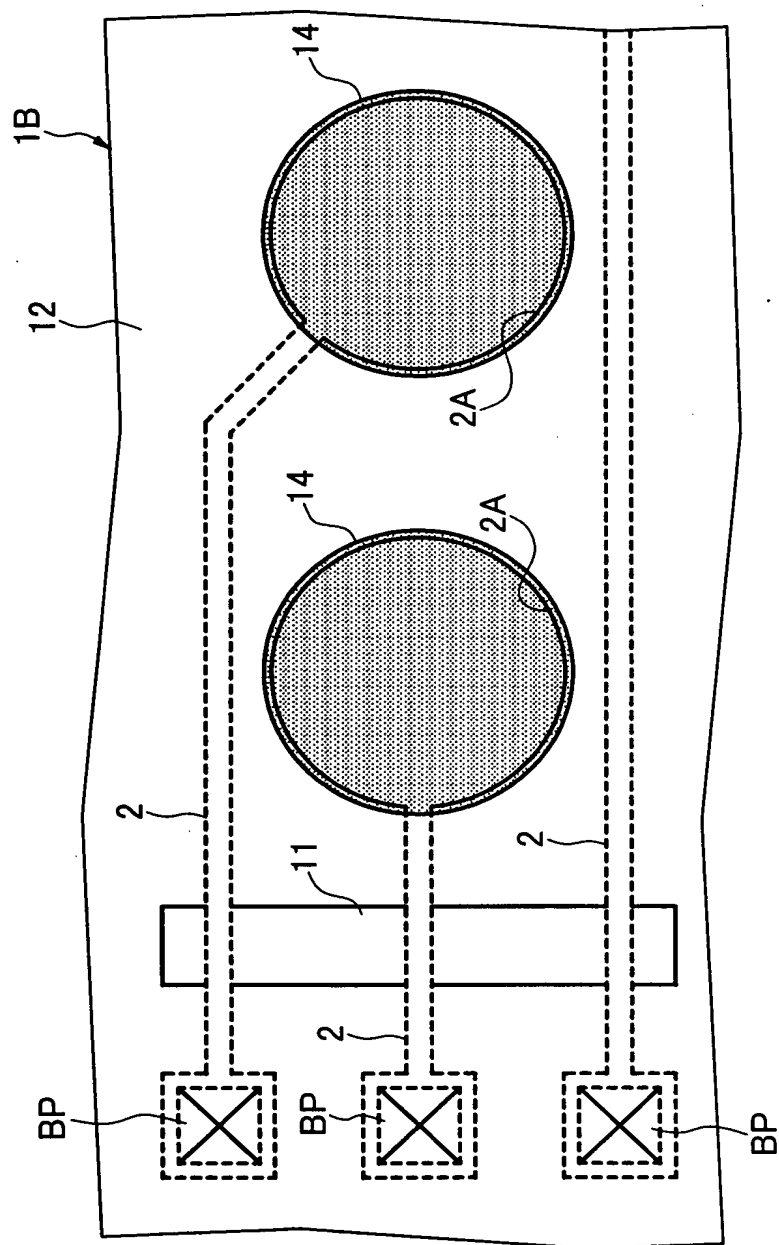
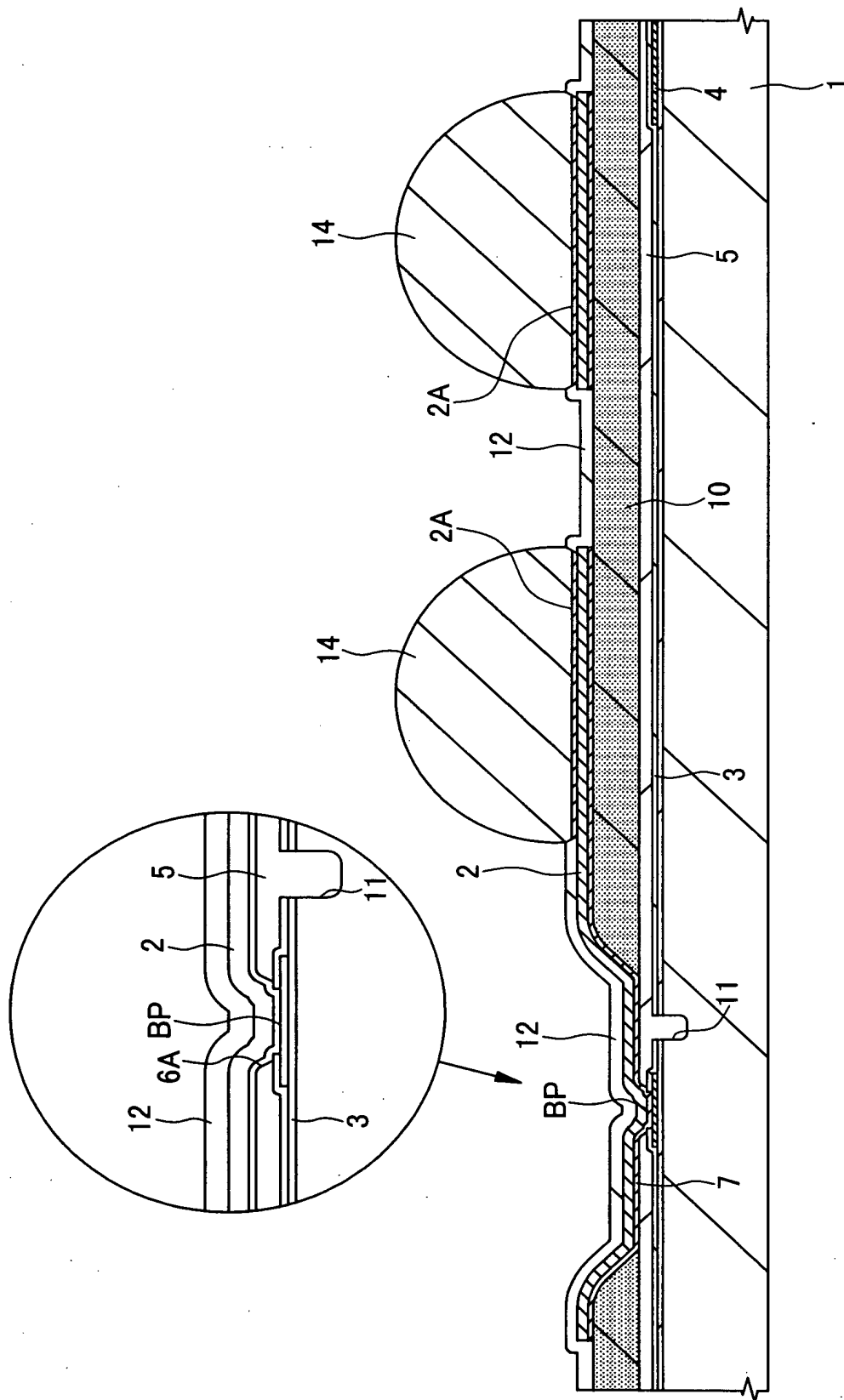


FIG.4



# FIG.5

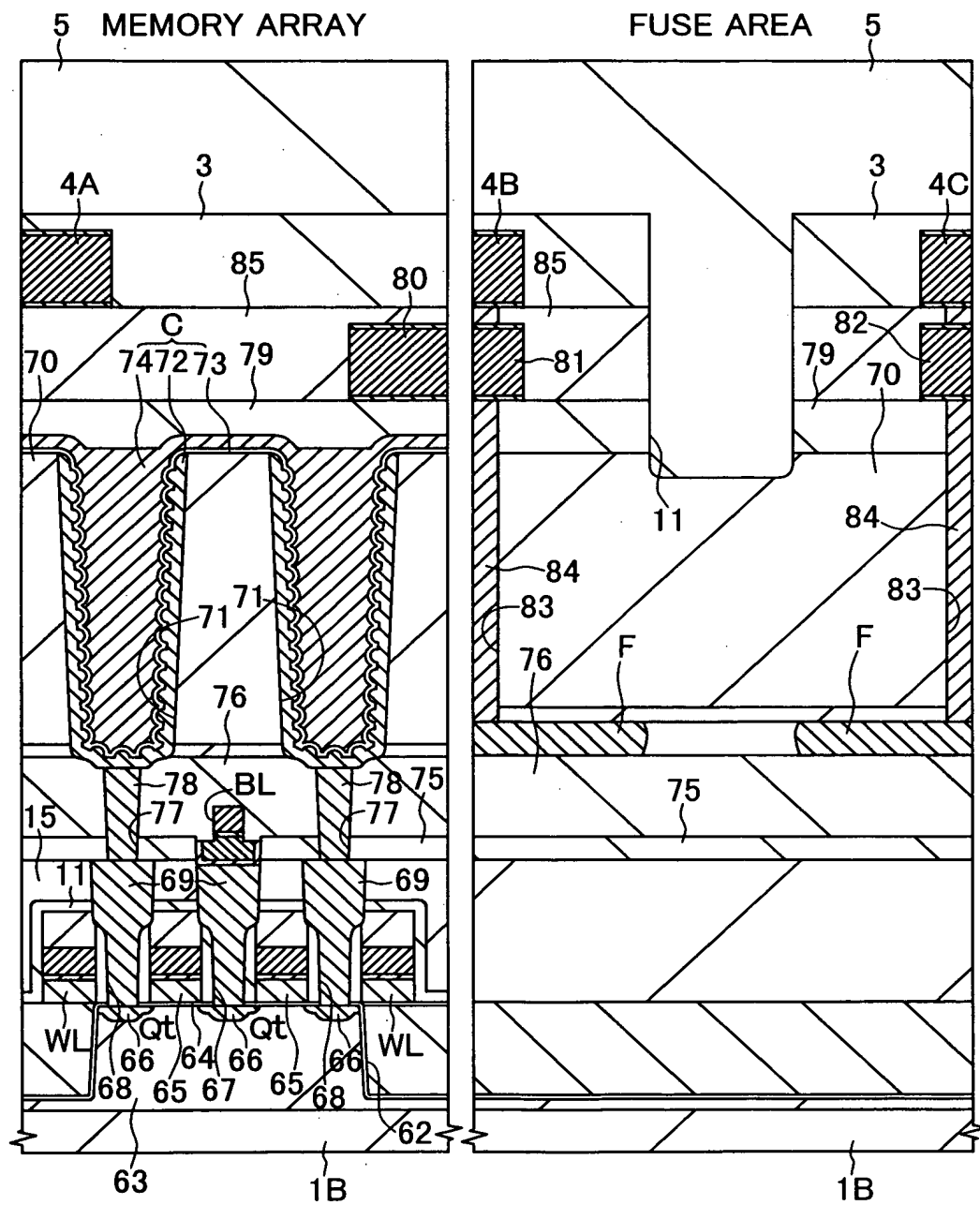


FIG.6

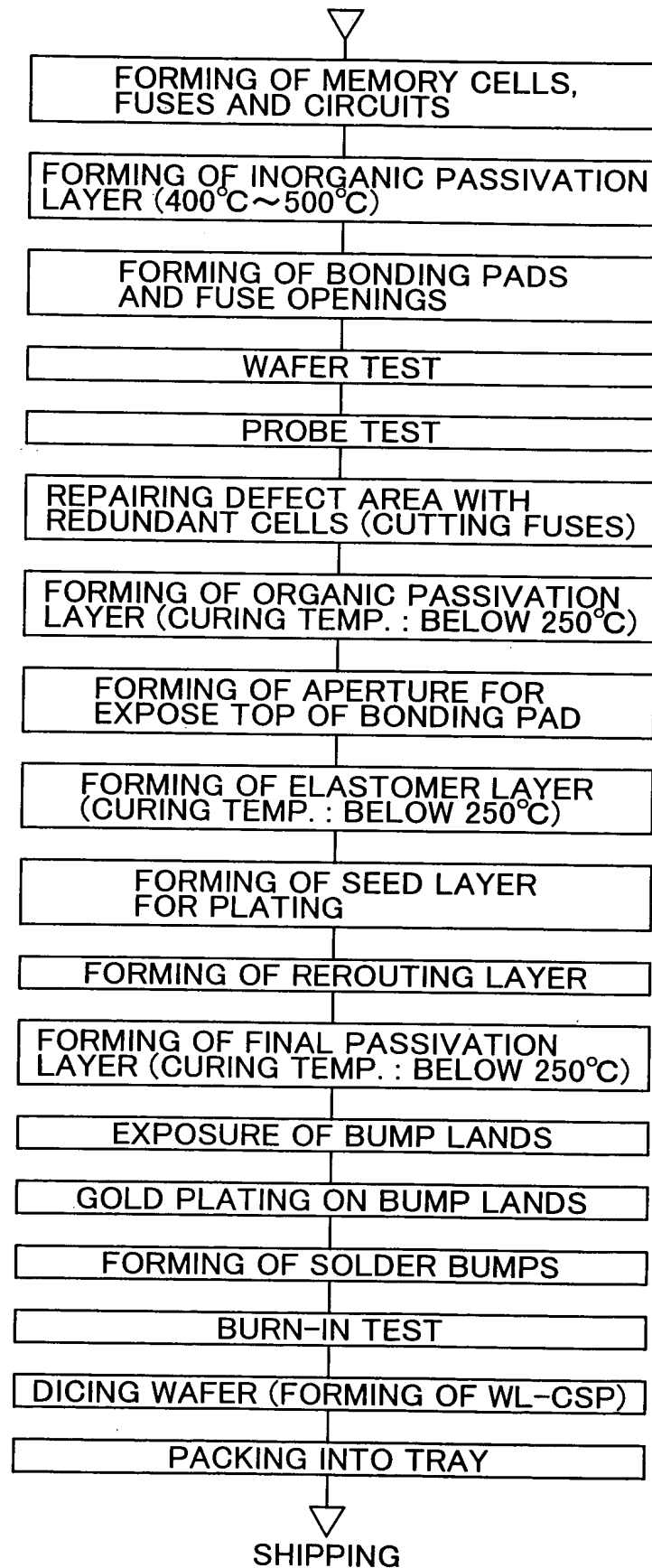


FIG.7

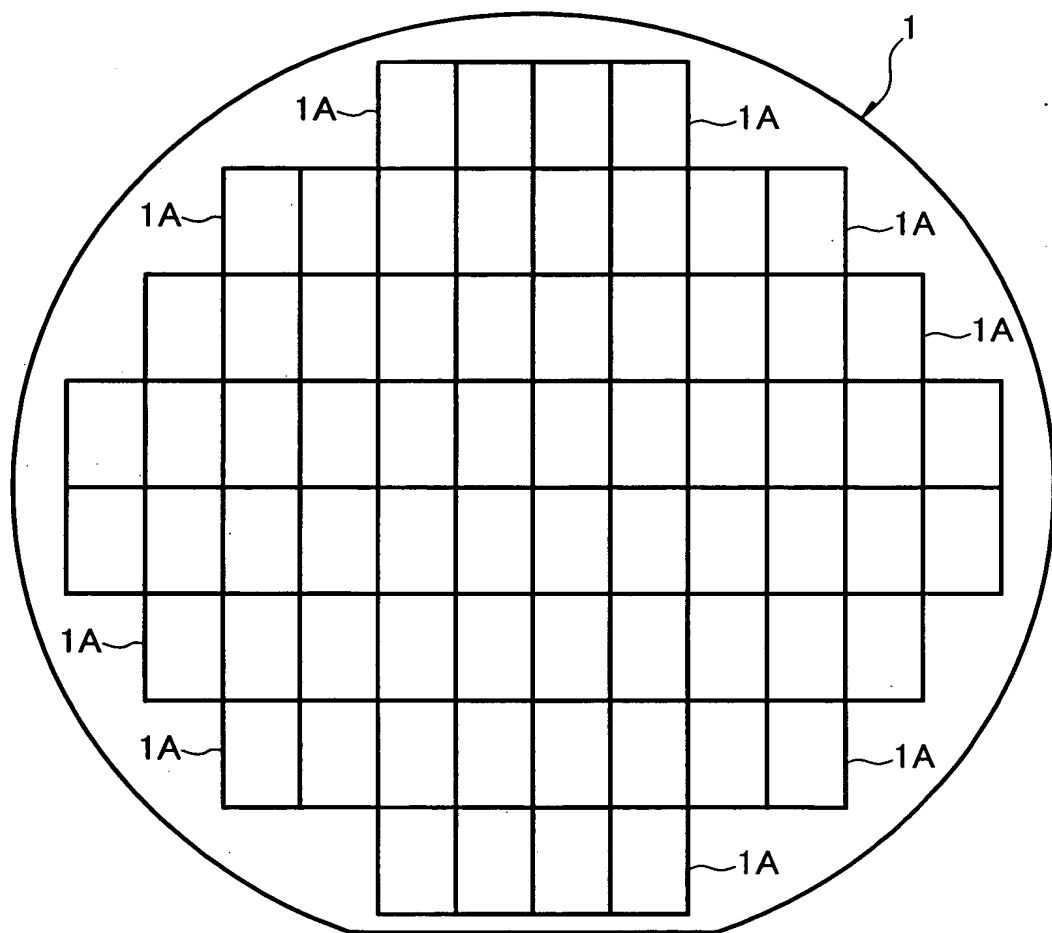
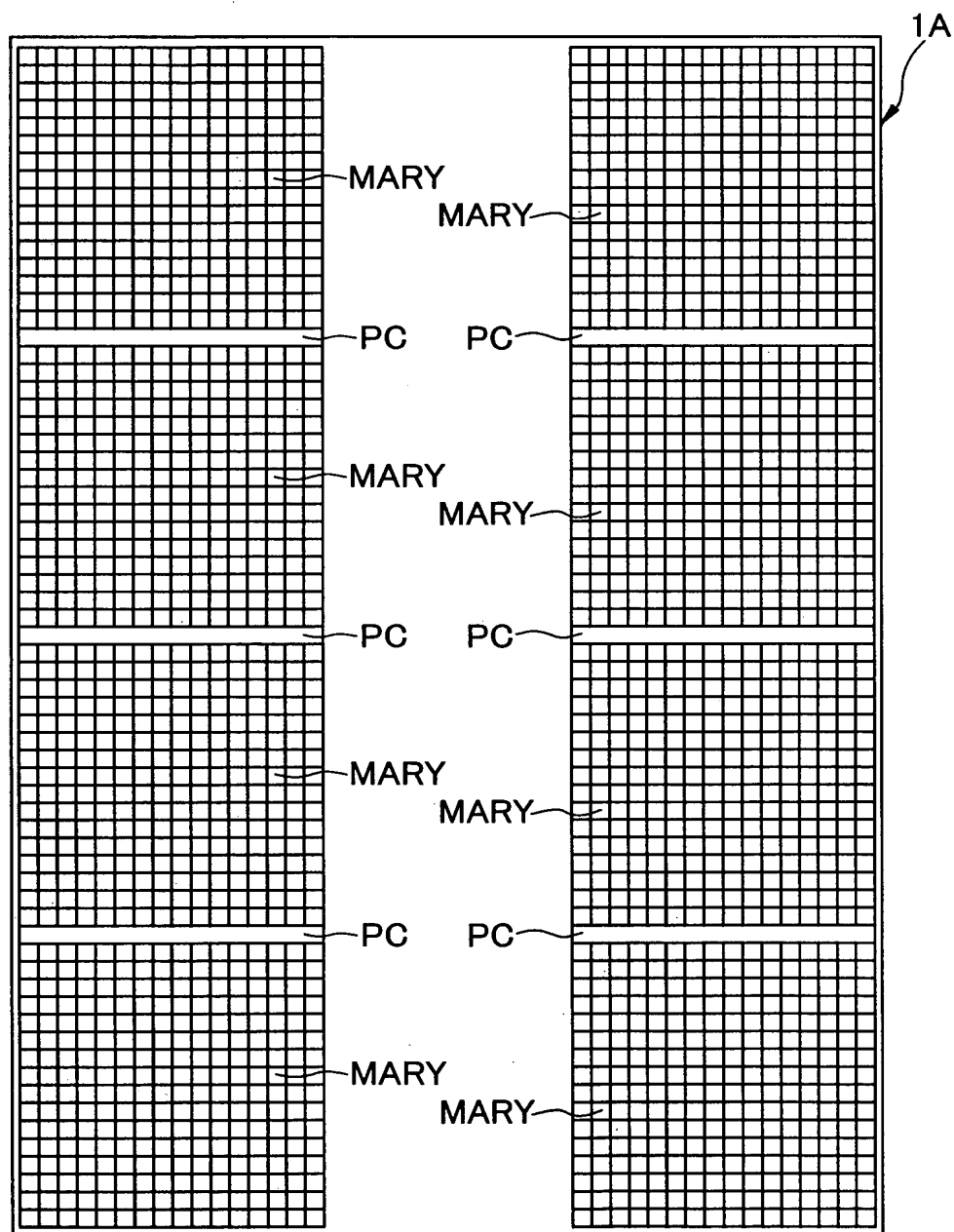


FIG.8

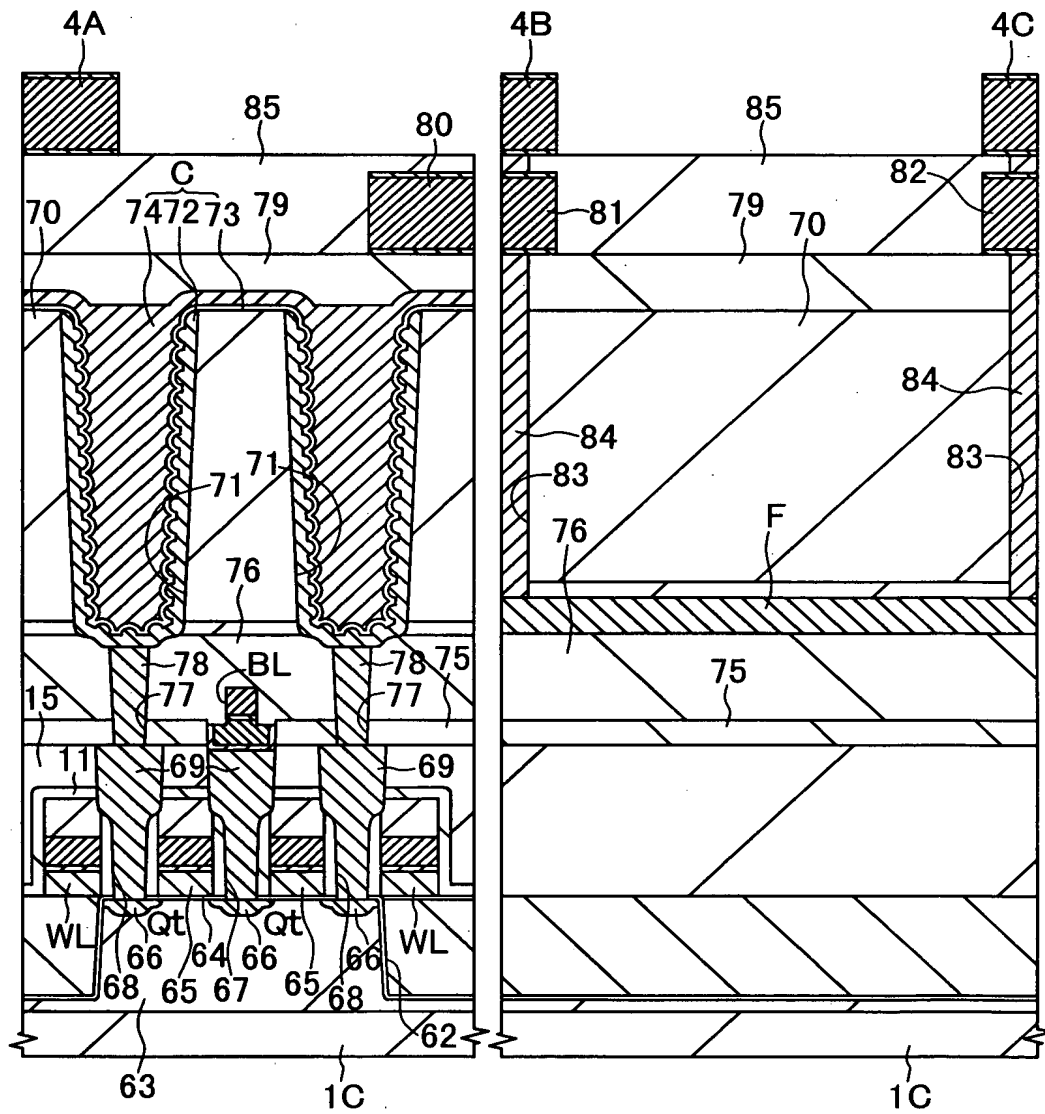




# FIG.9

MEMORY ARRAY

FUSE AREA



# FIG.10

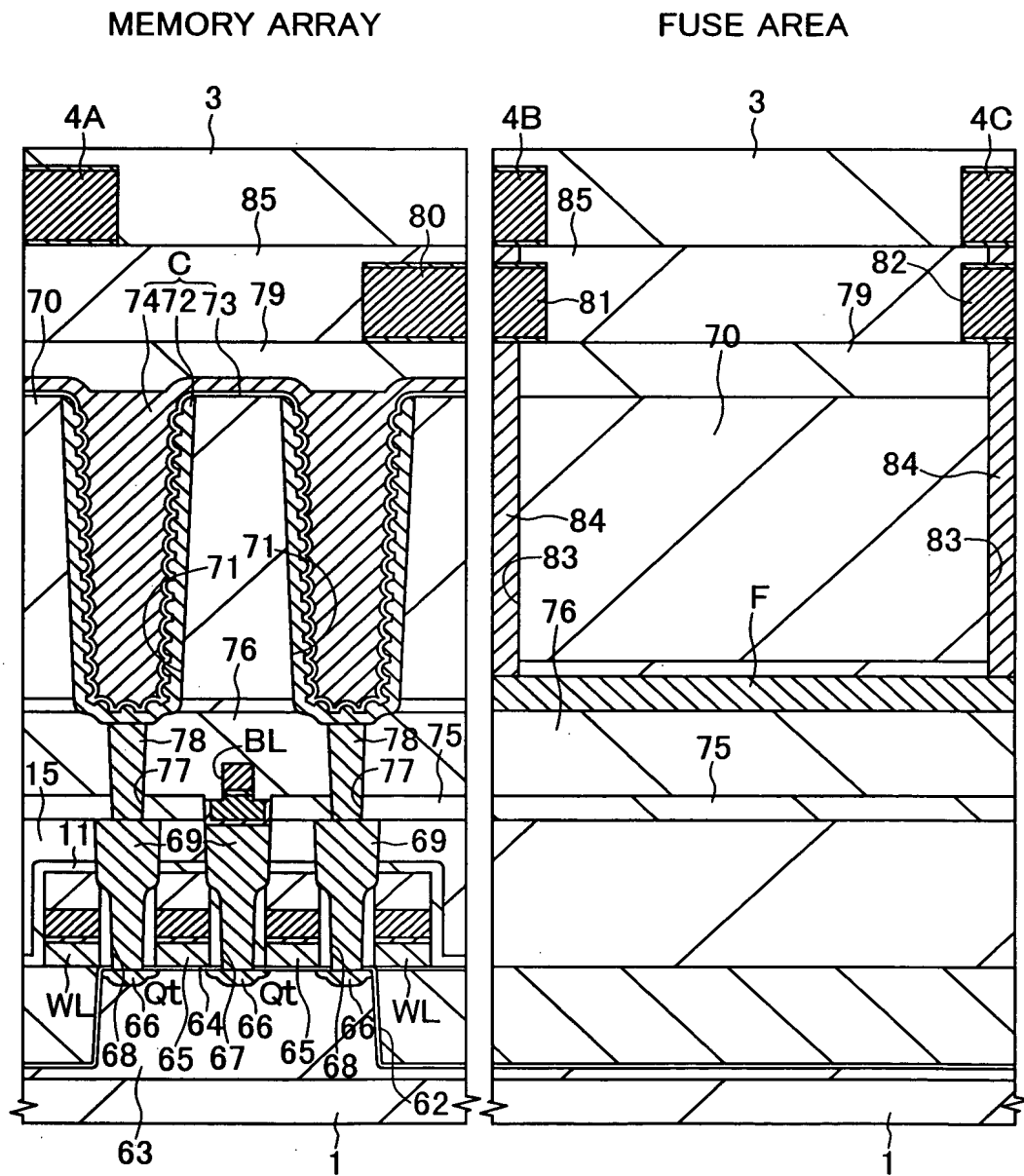
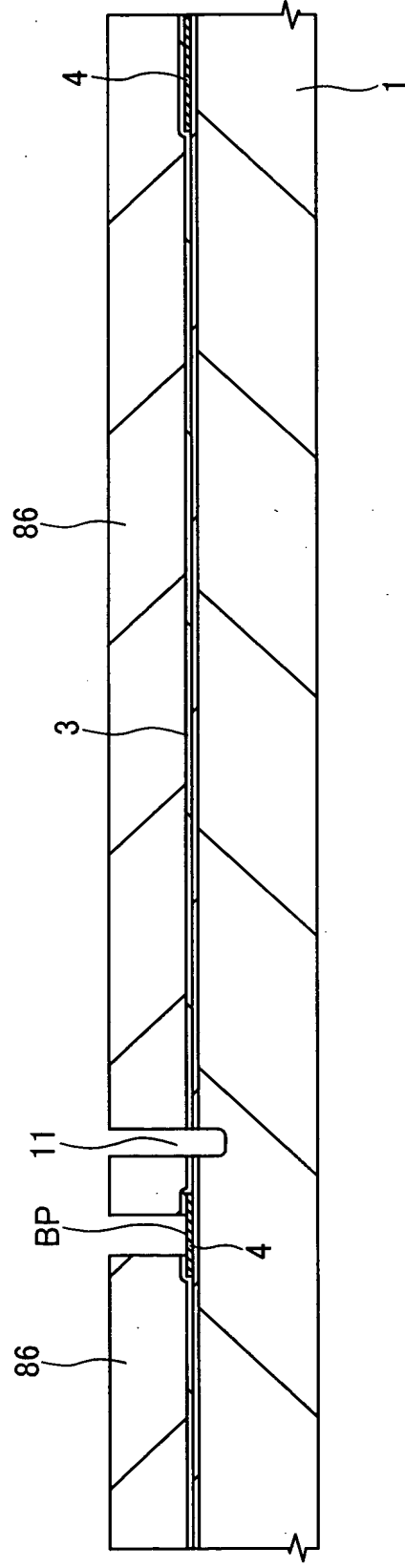


FIG.11



# FIG.12

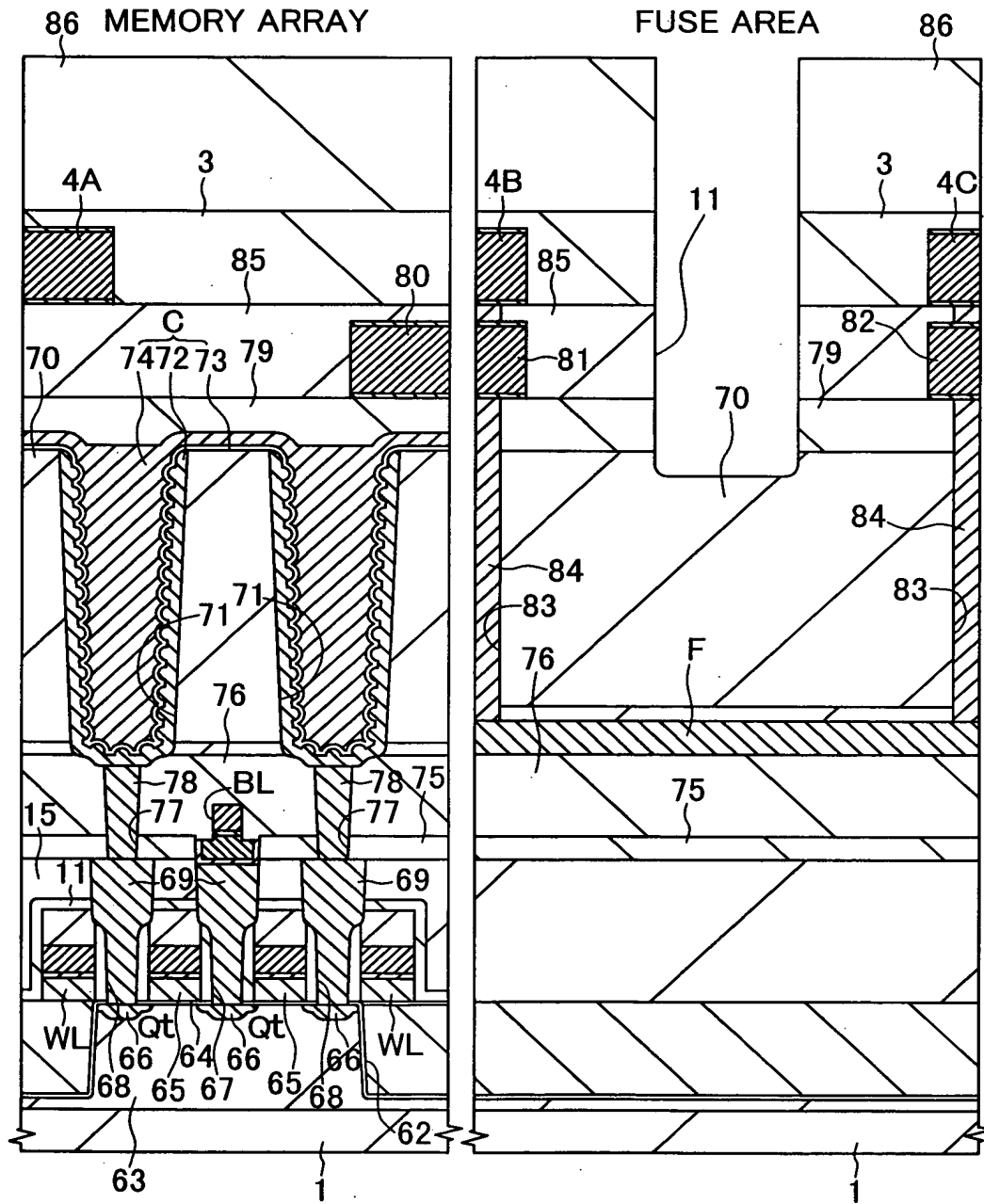
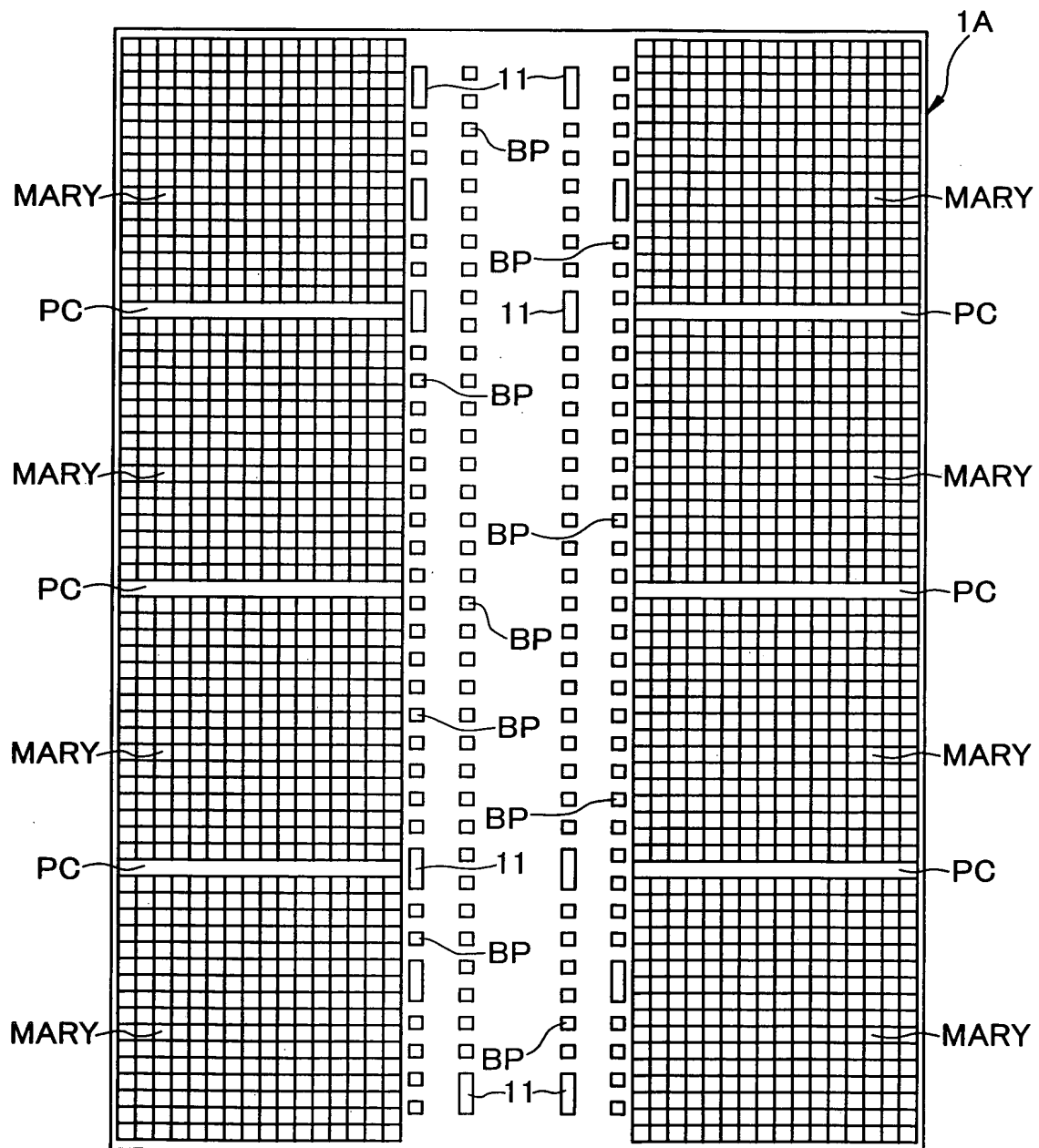


FIG.13



# FIG.14

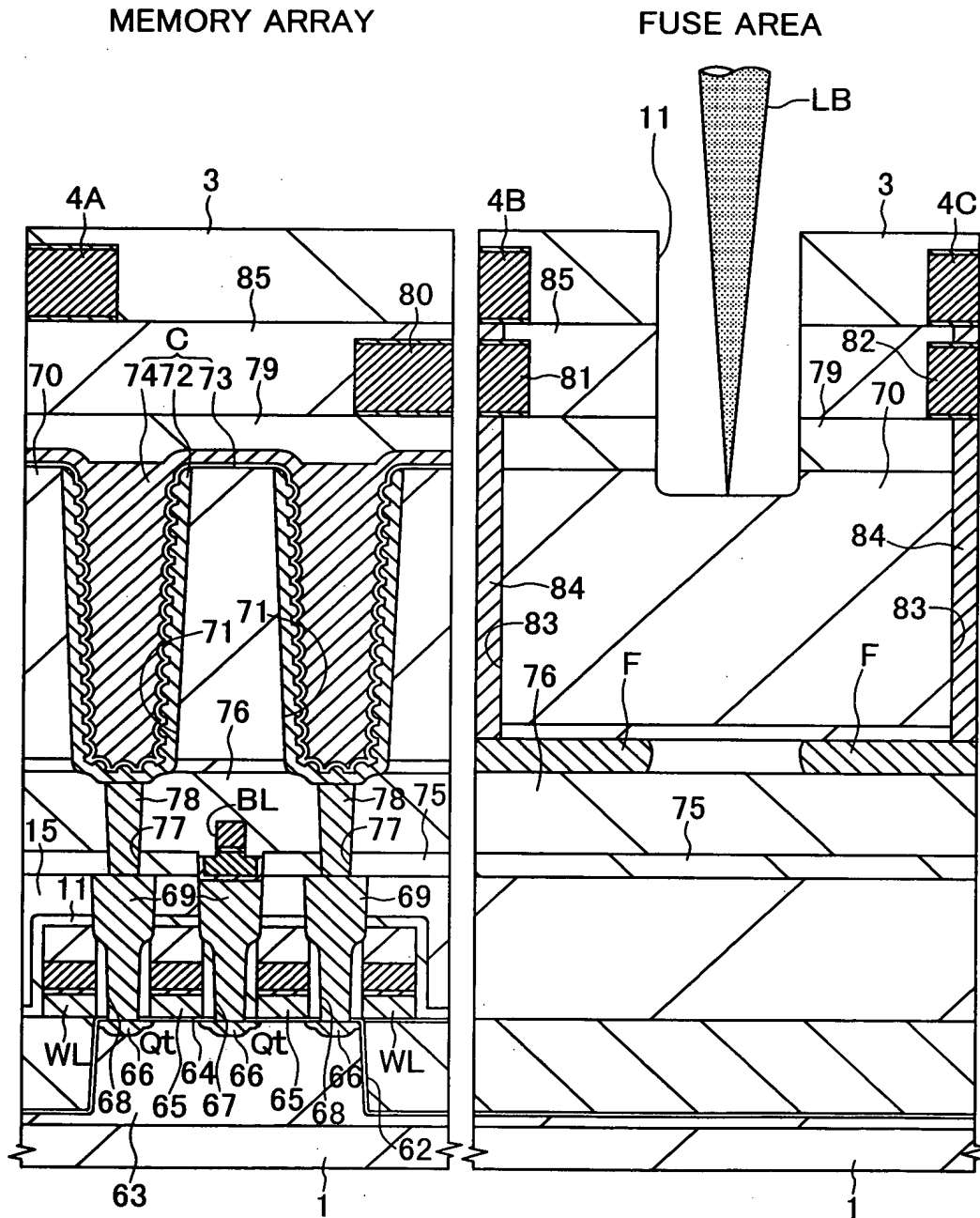
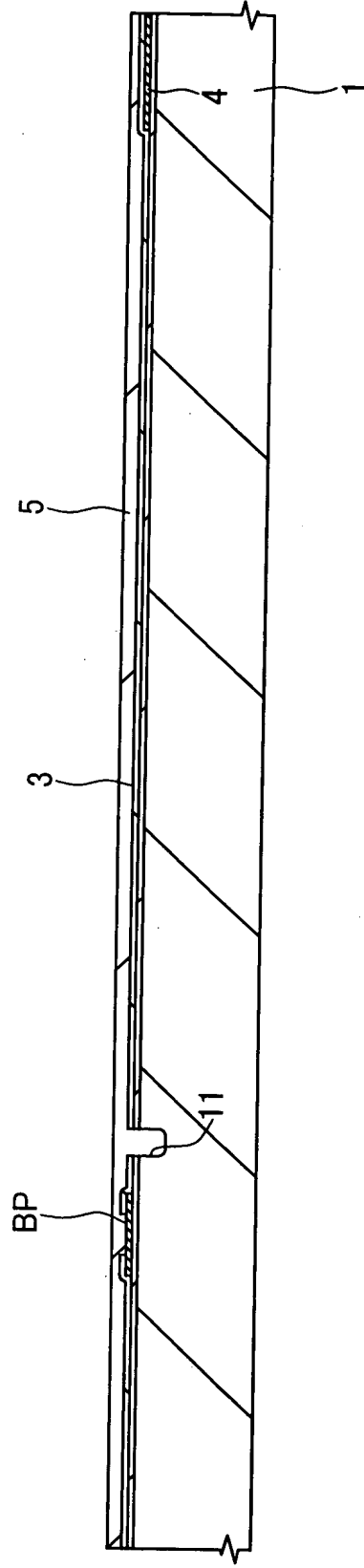


FIG.15



# FIG.16

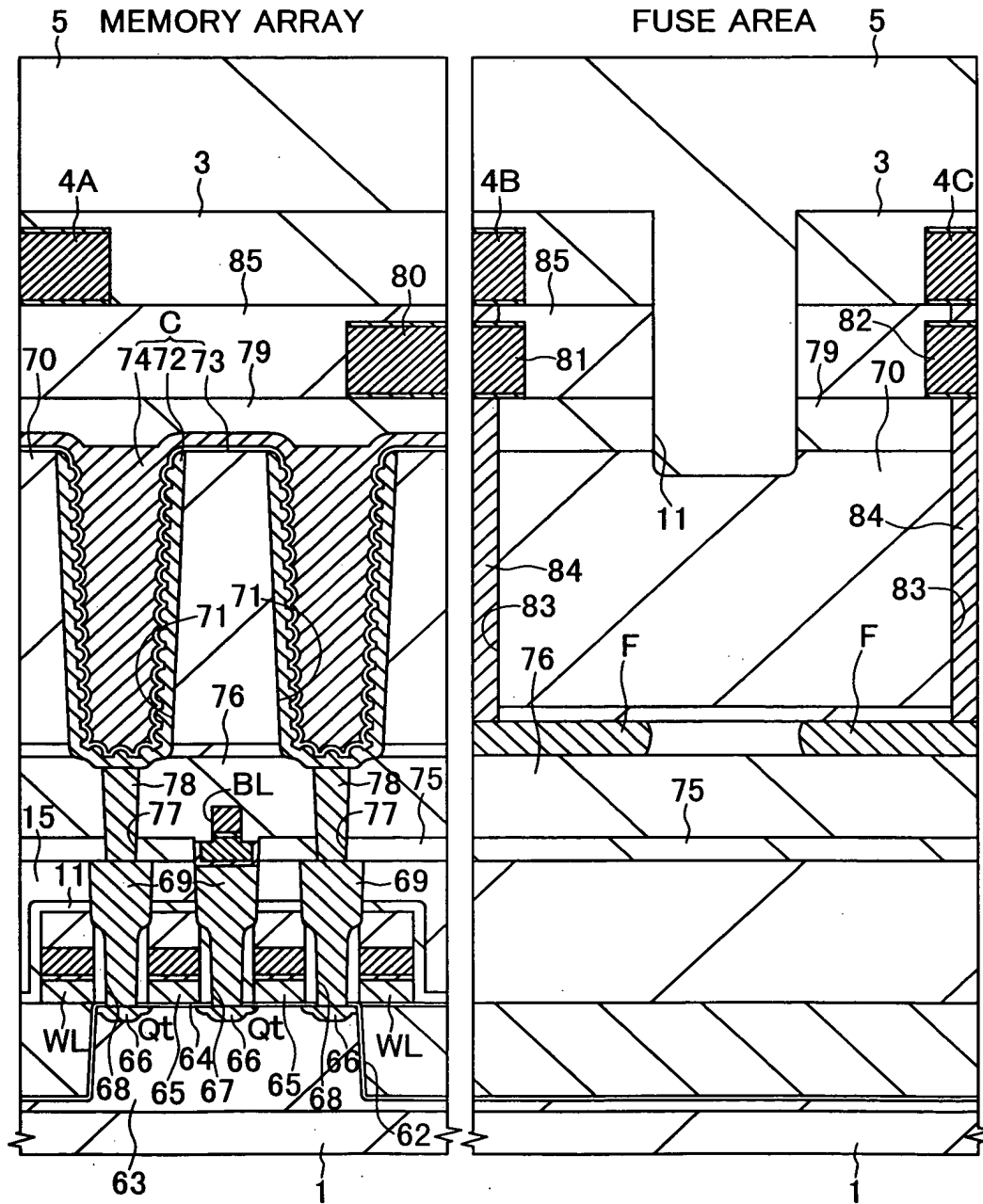




FIG.17

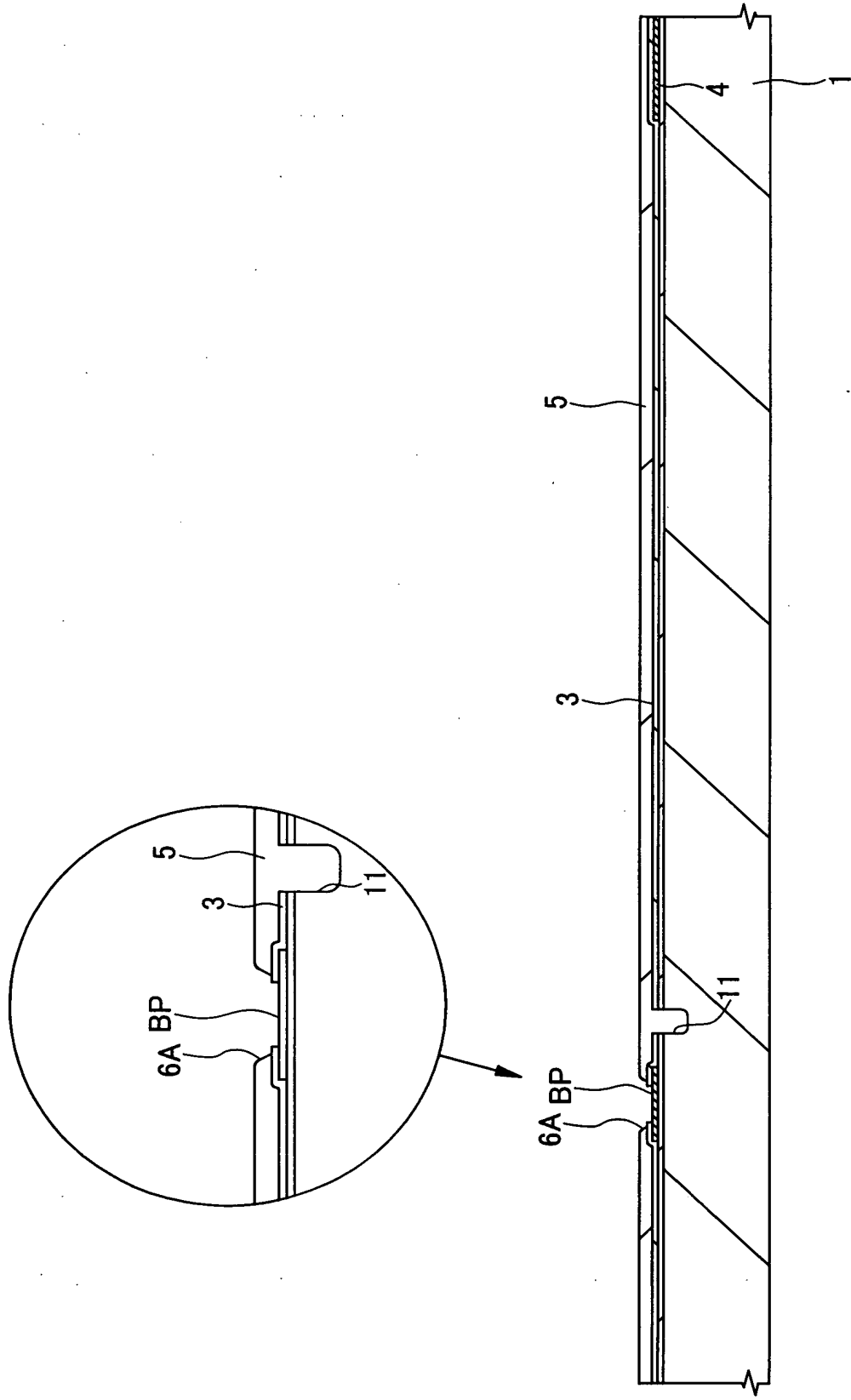


FIG.18

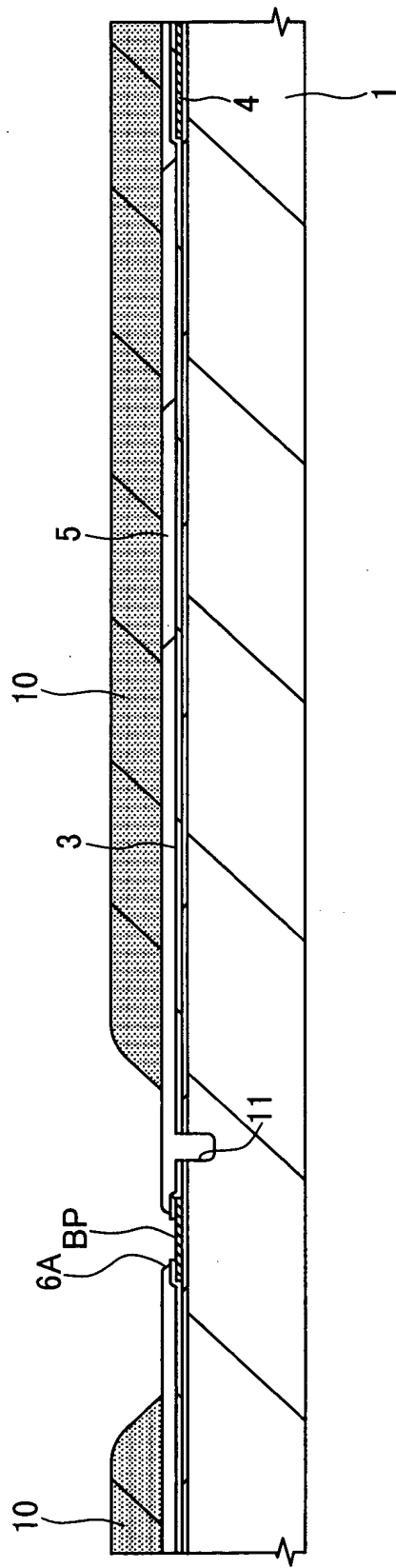


FIG.19

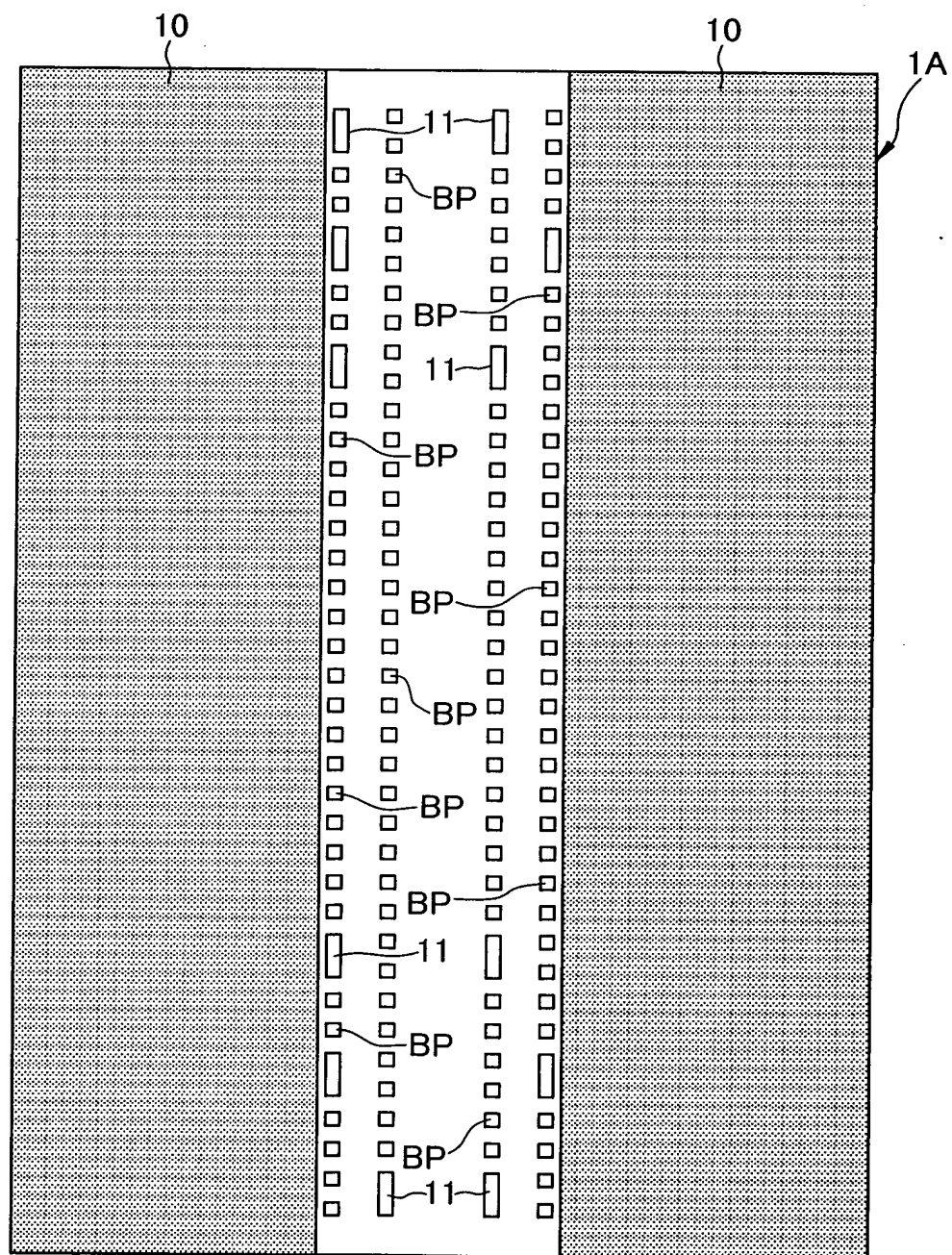


FIG.20

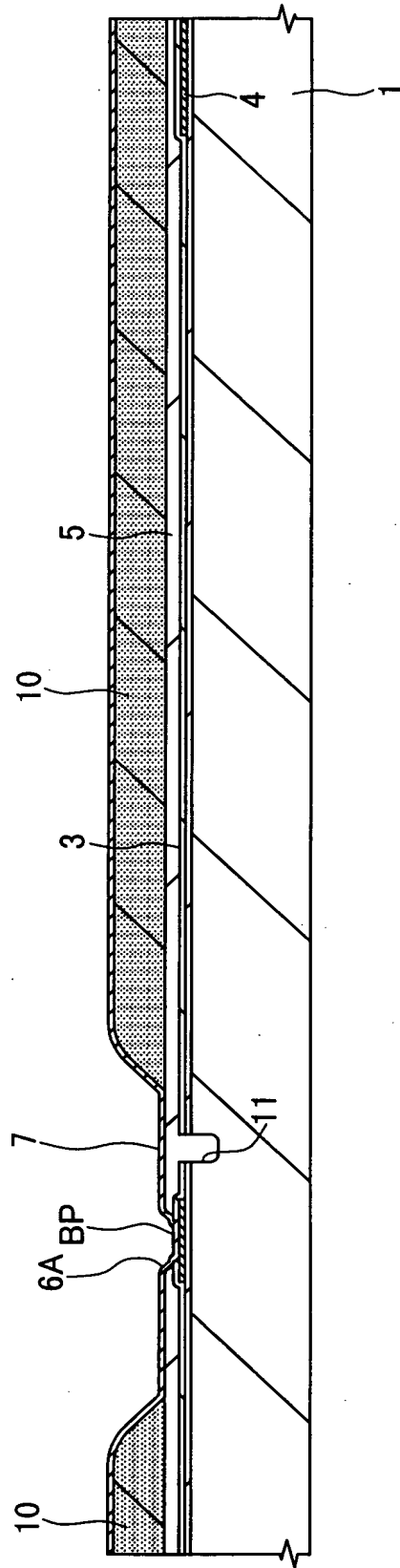


FIG.21

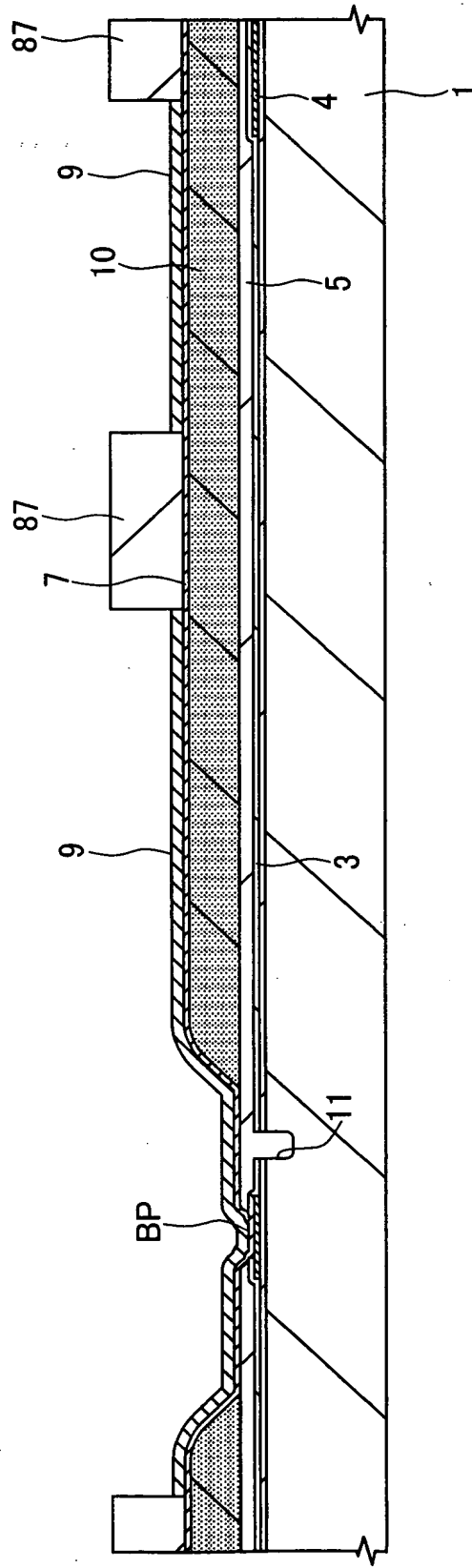


FIG.22

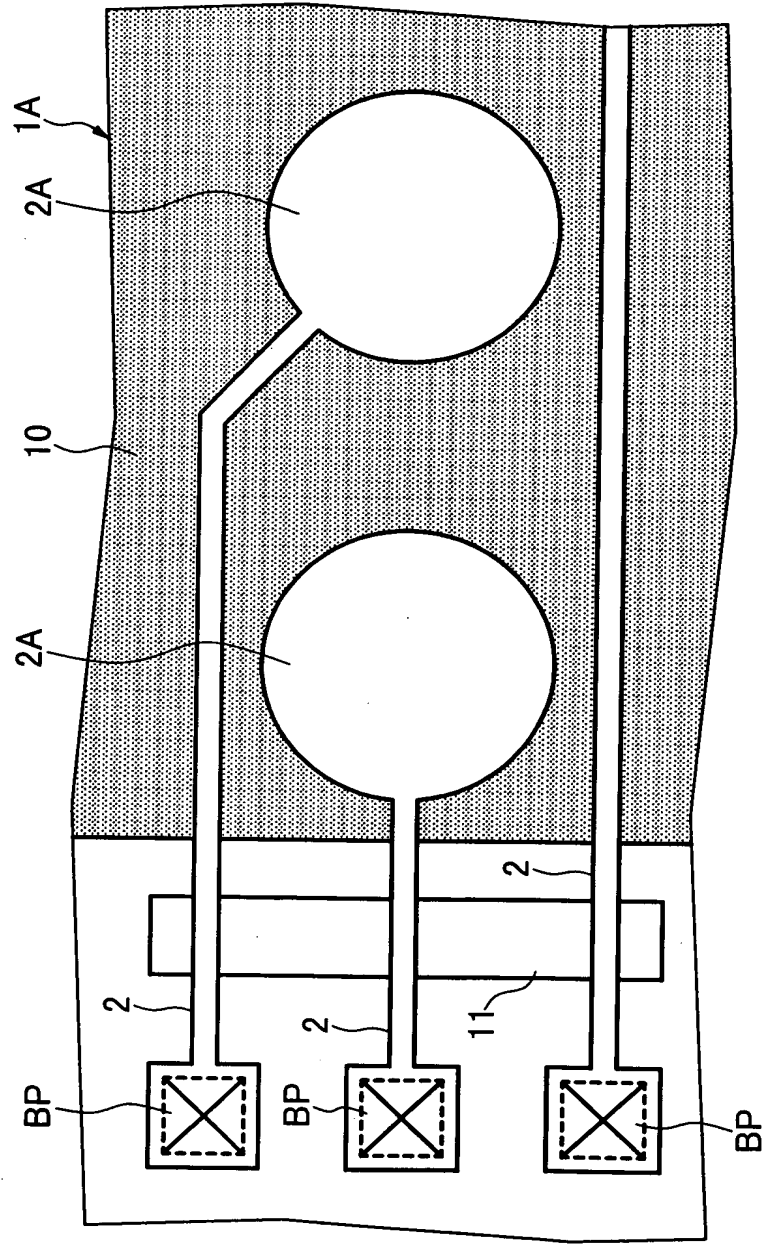


FIG.23

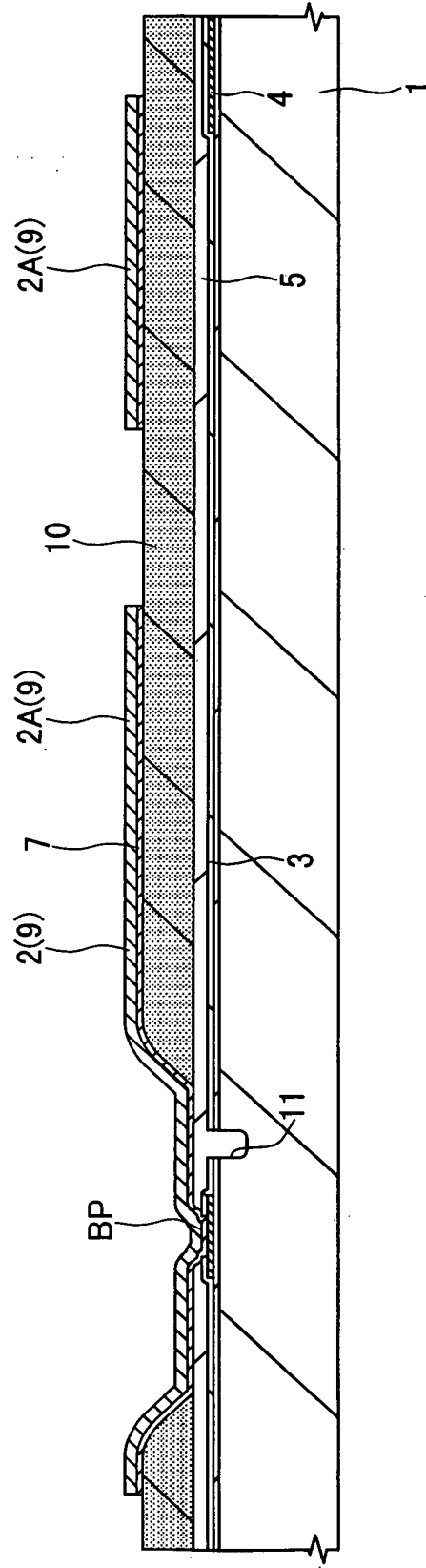


FIG.24

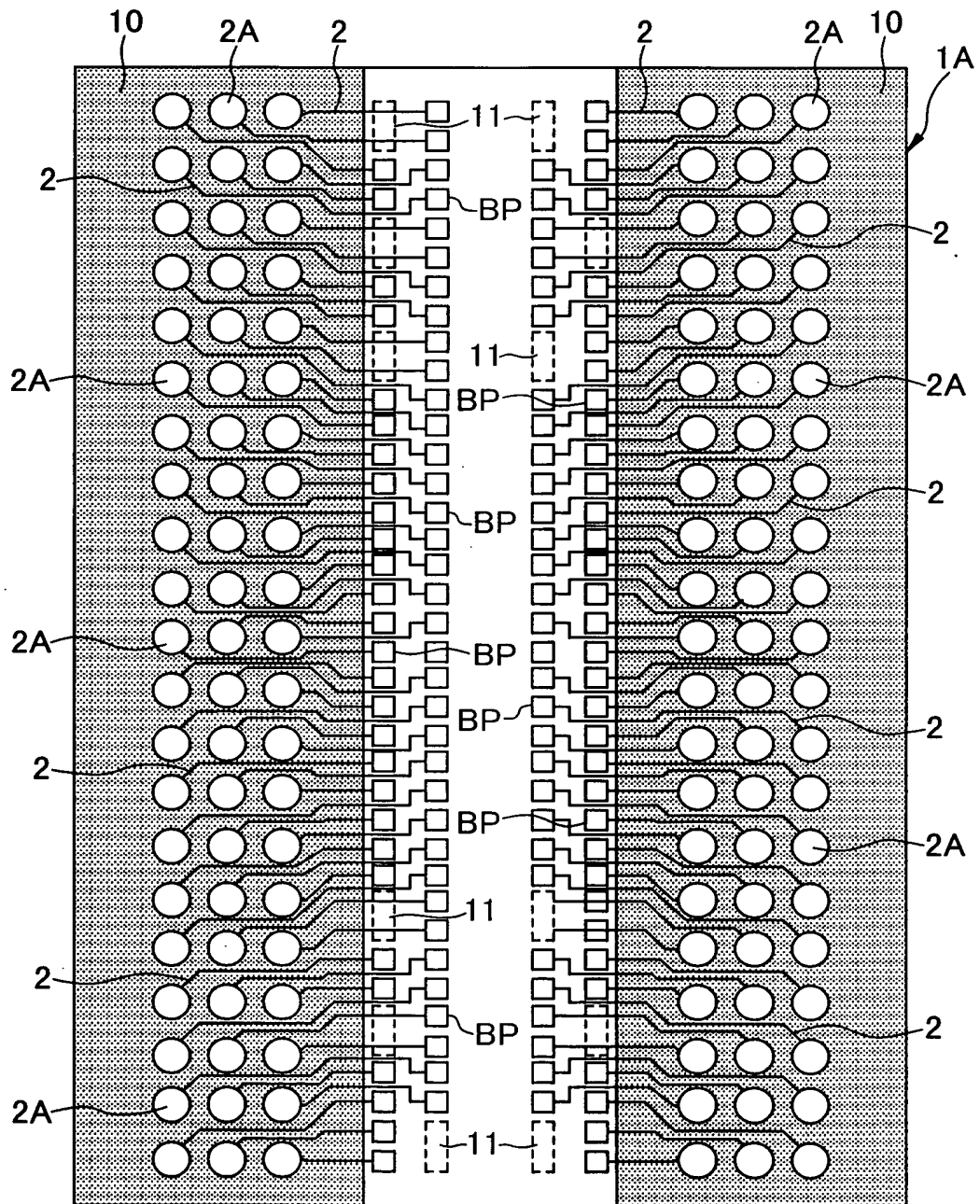




FIG.25

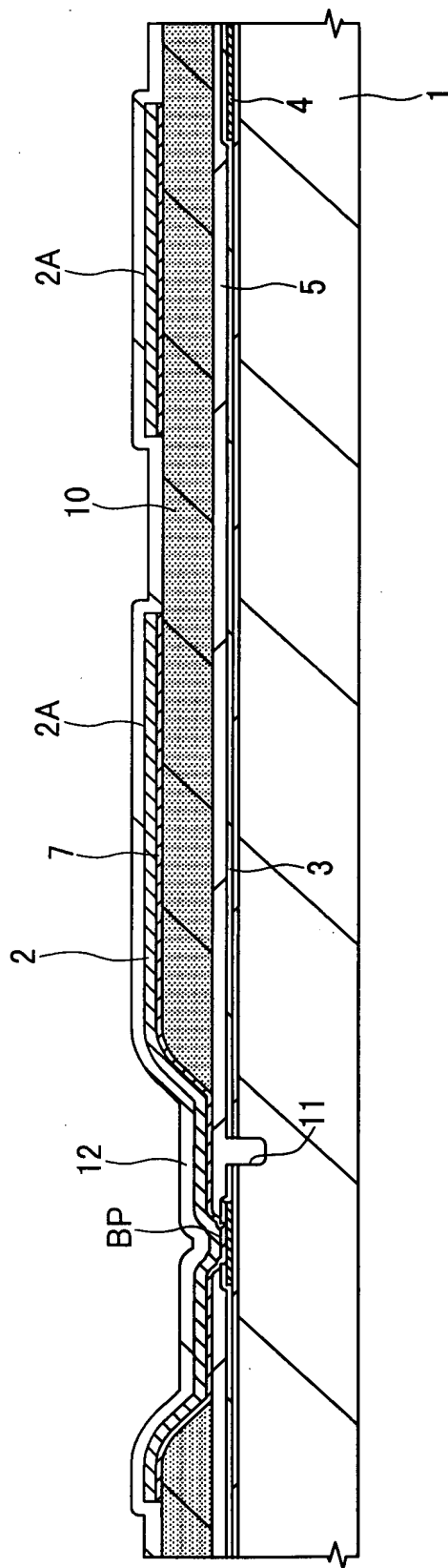


FIG.26

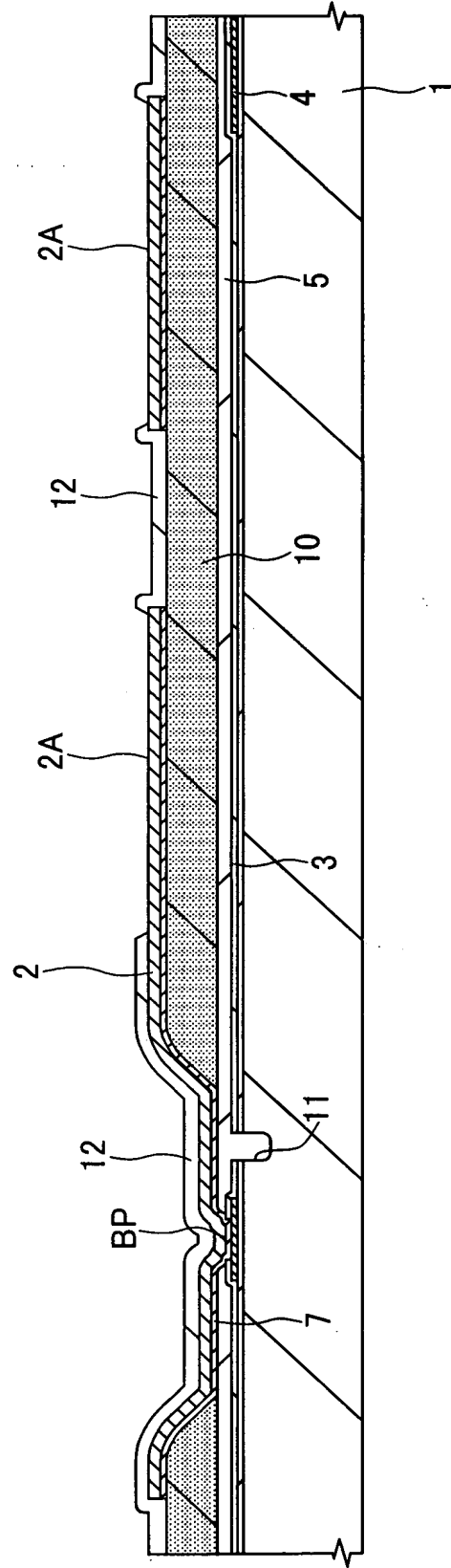
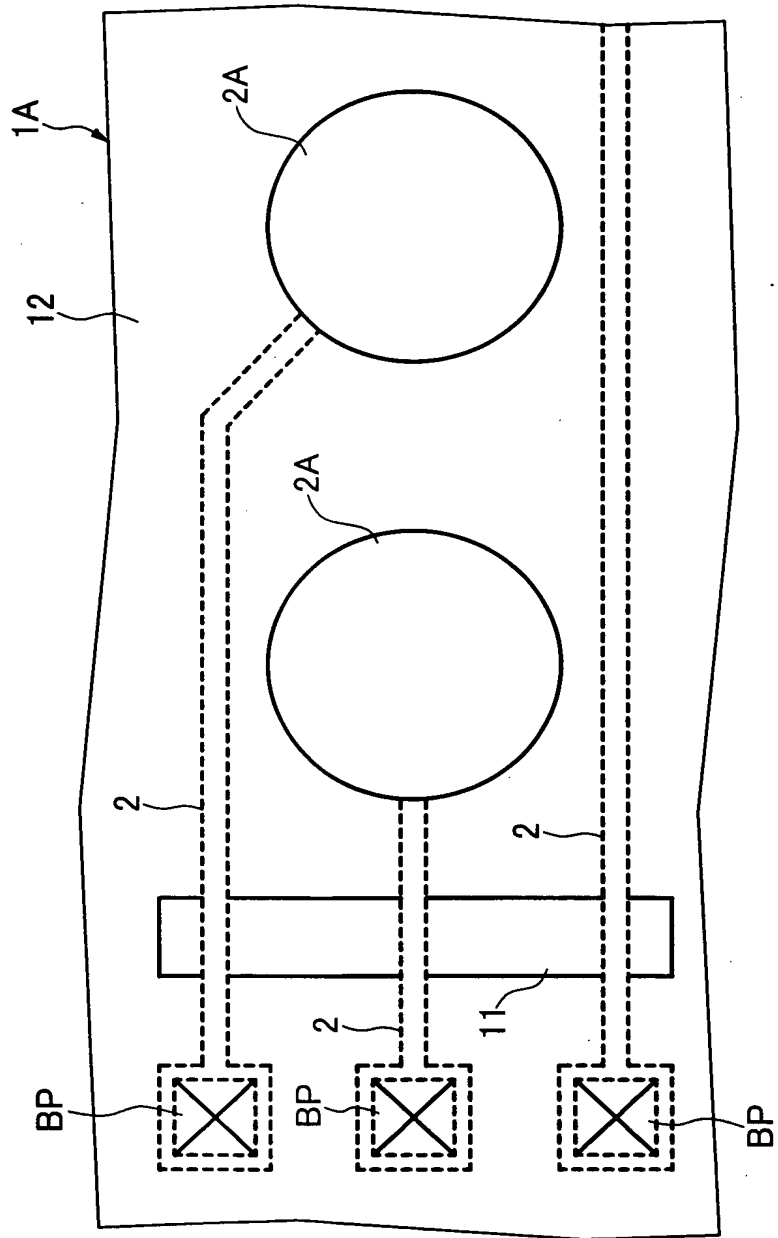


FIG.27



# FIG. 28

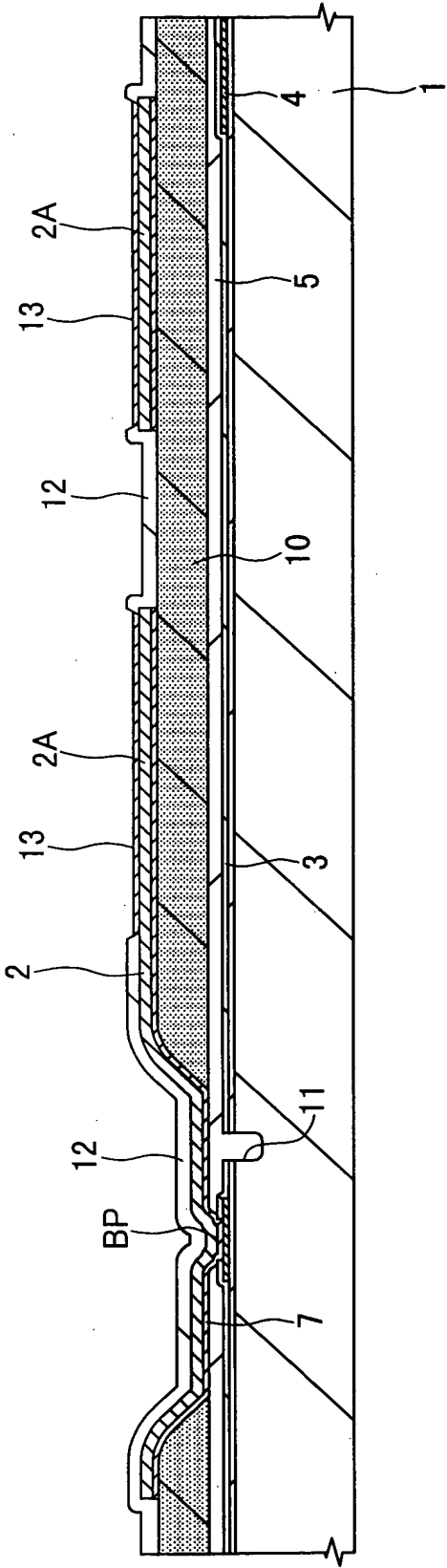


FIG.29

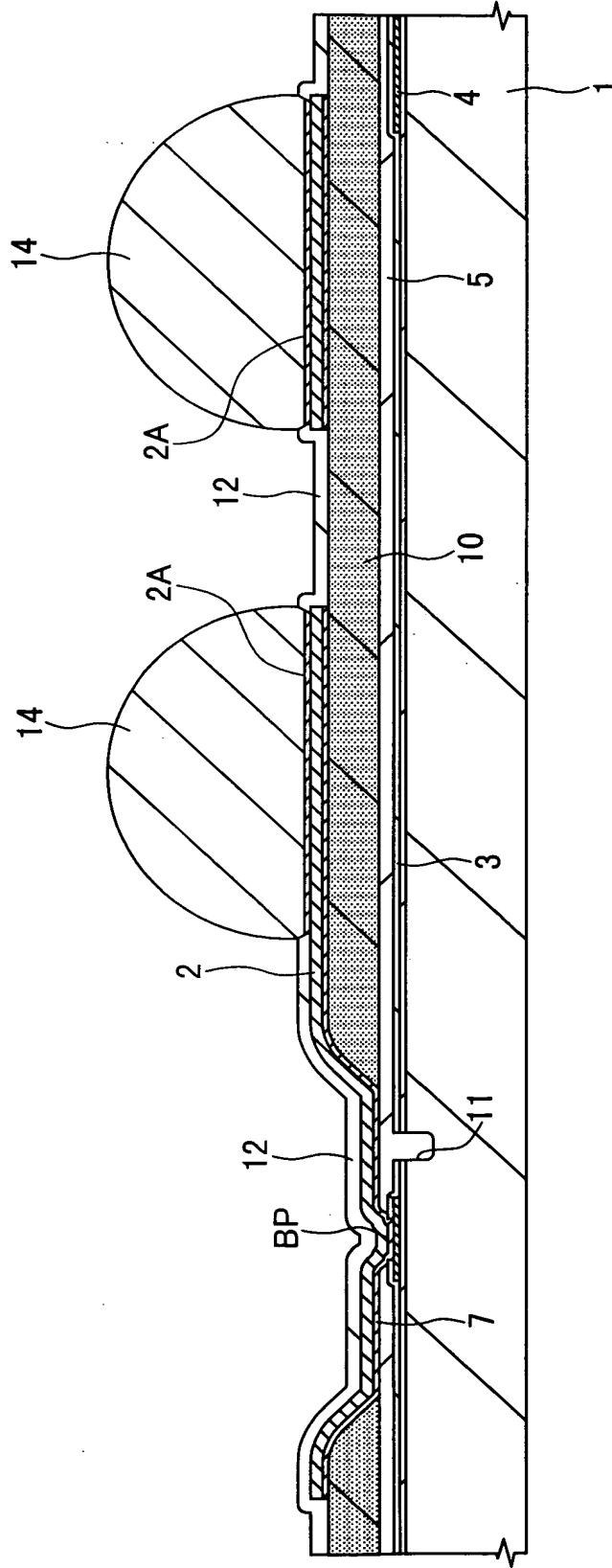
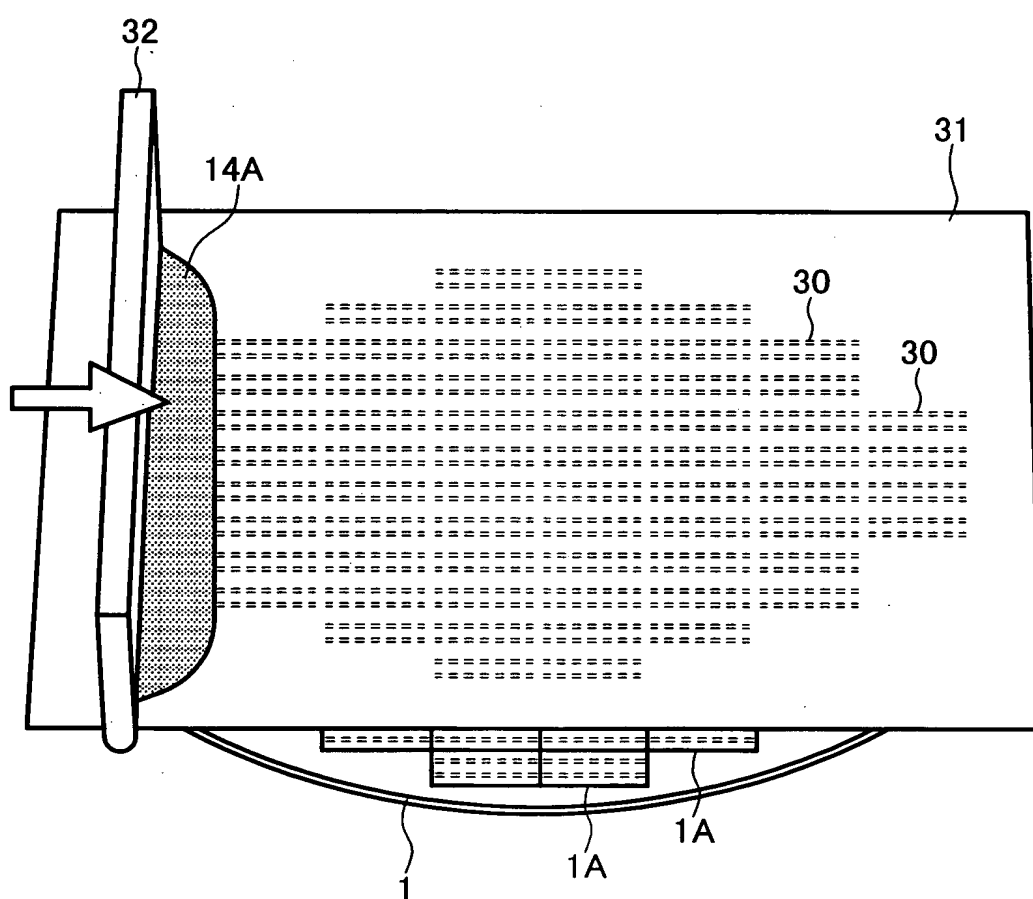


FIG.30



**FIG. 31**

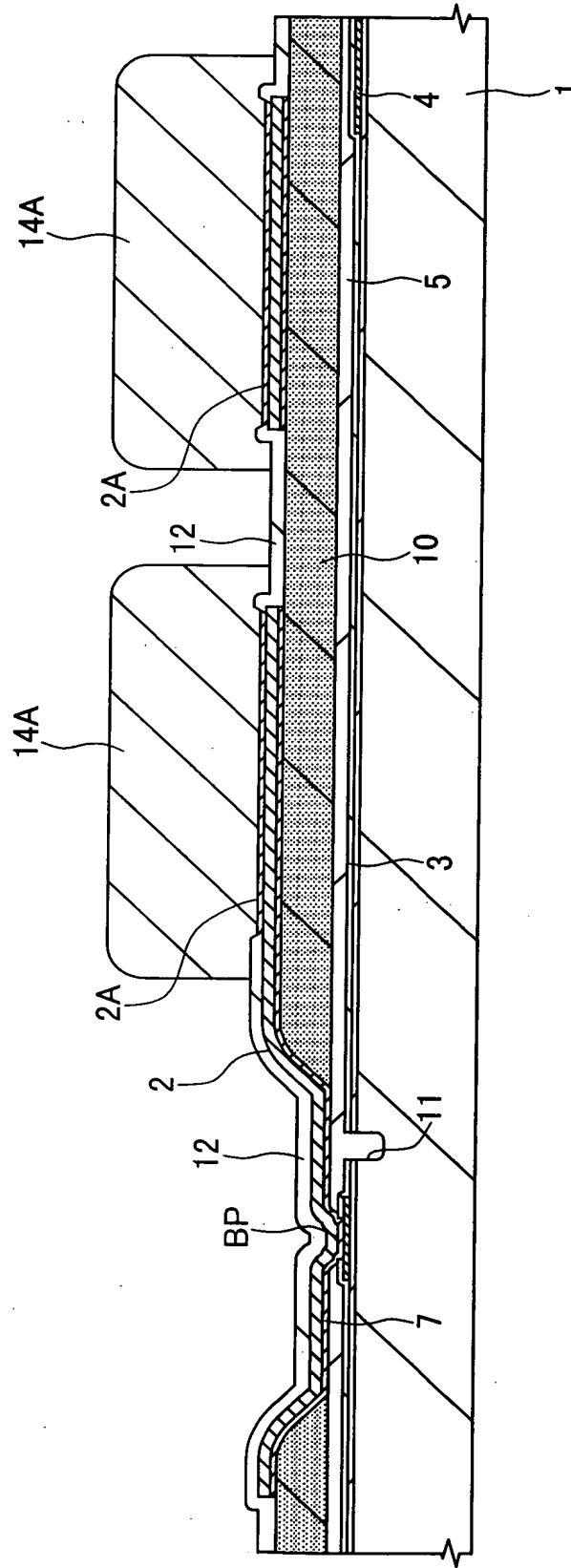


FIG.32

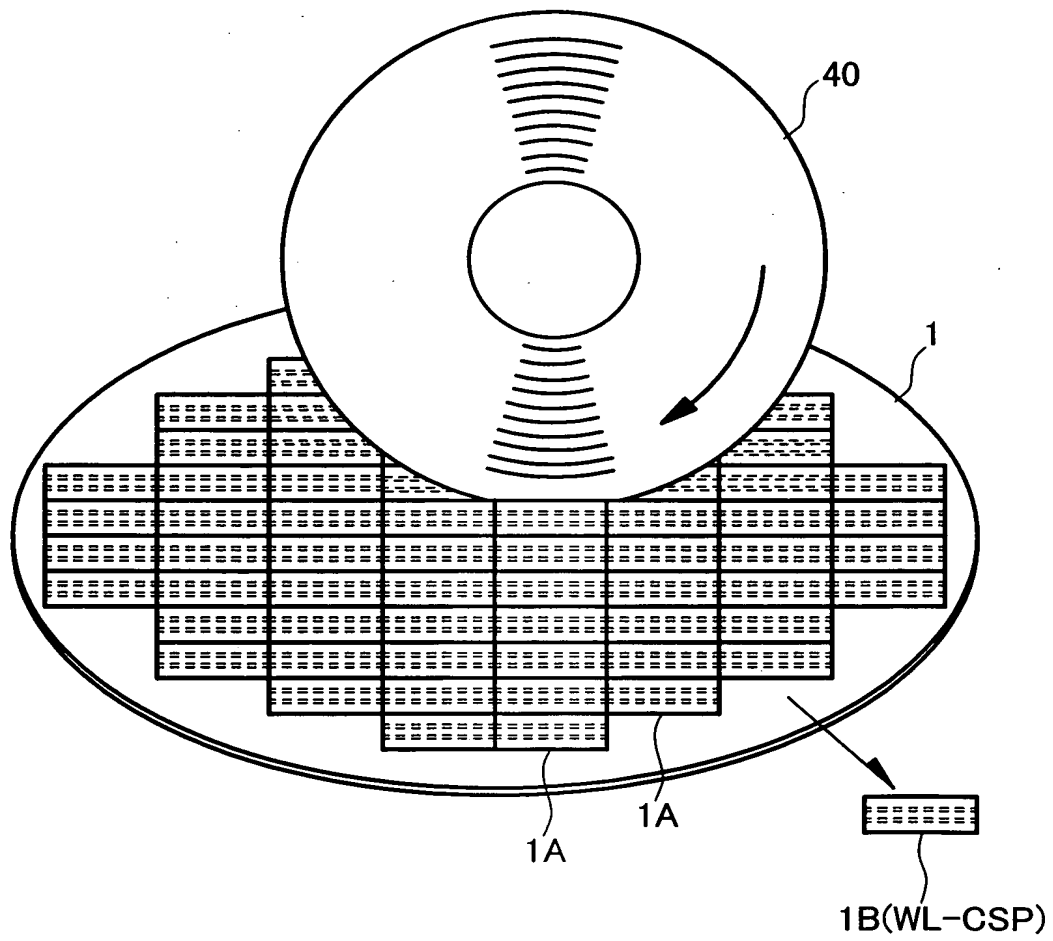




FIG.33

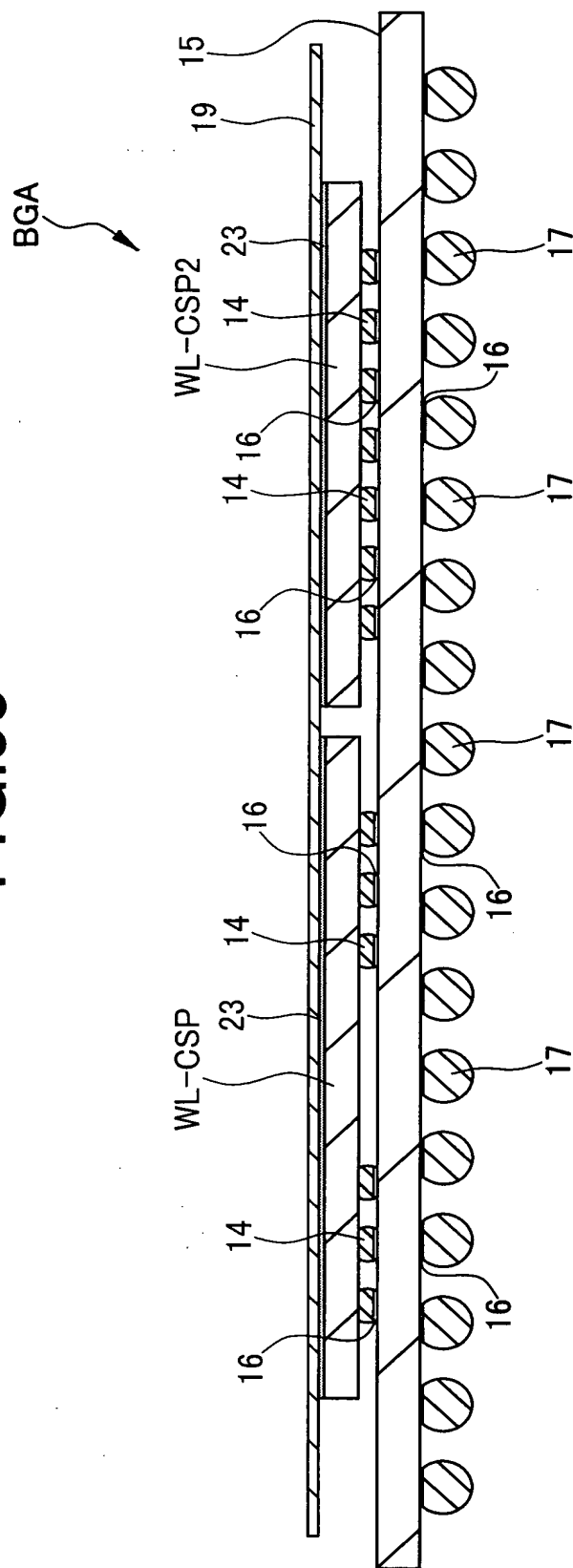
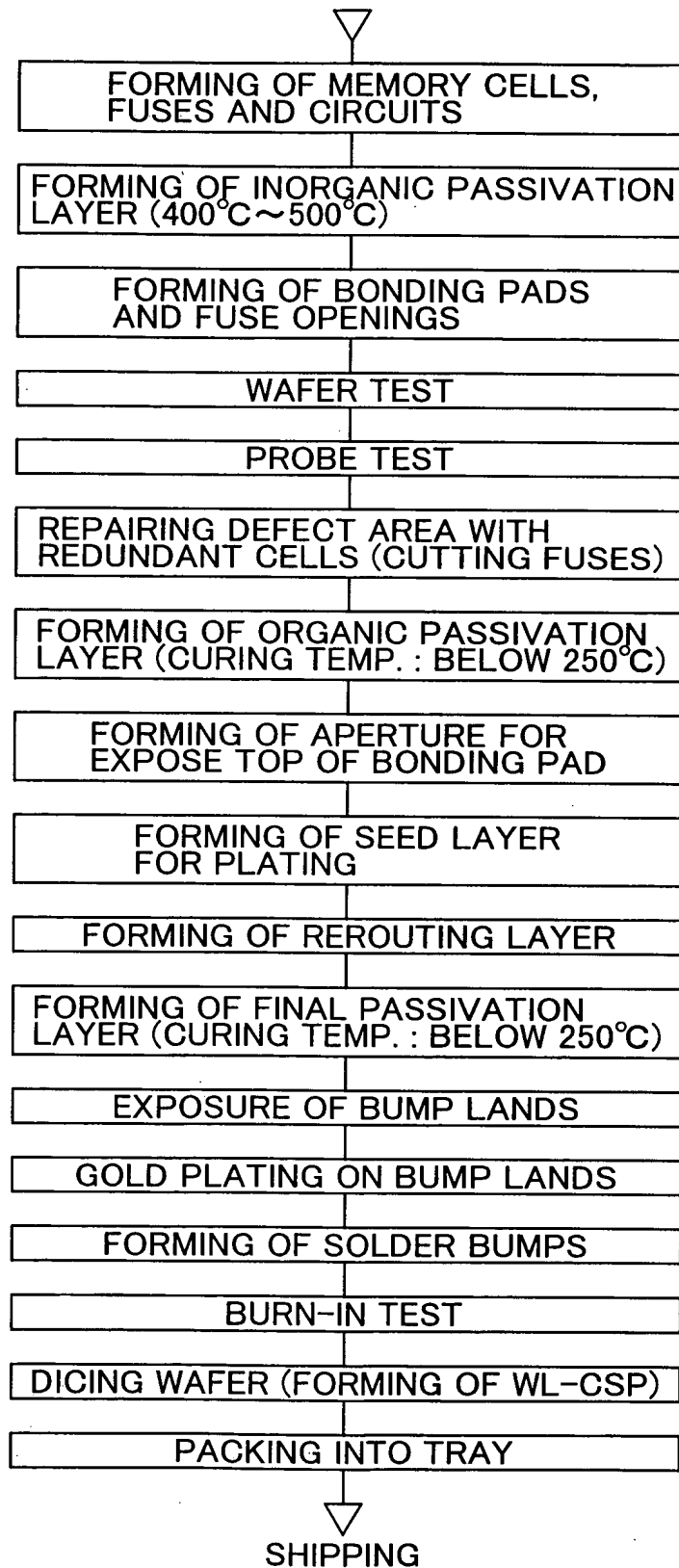


FIG.34



**FIG.35**

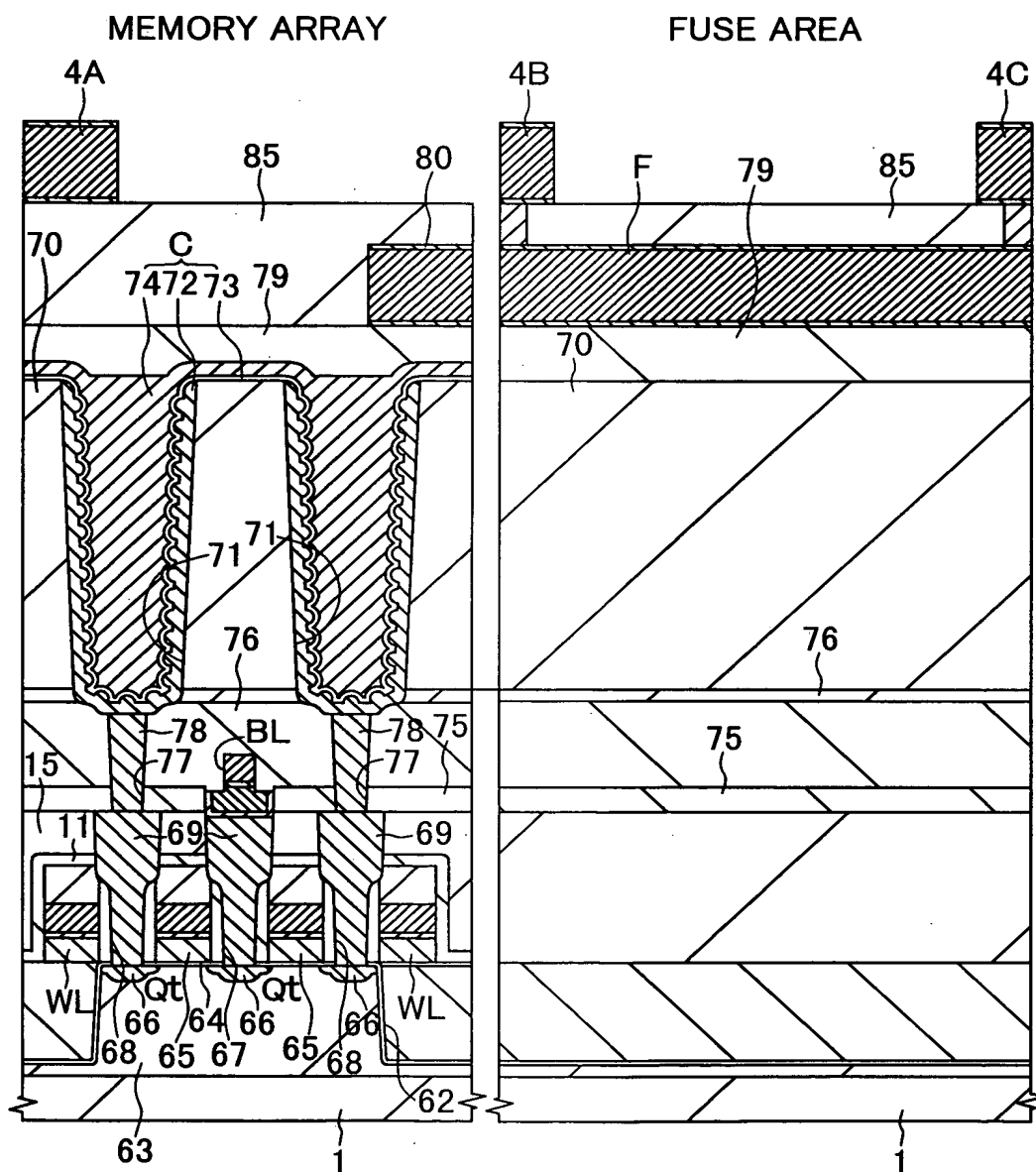
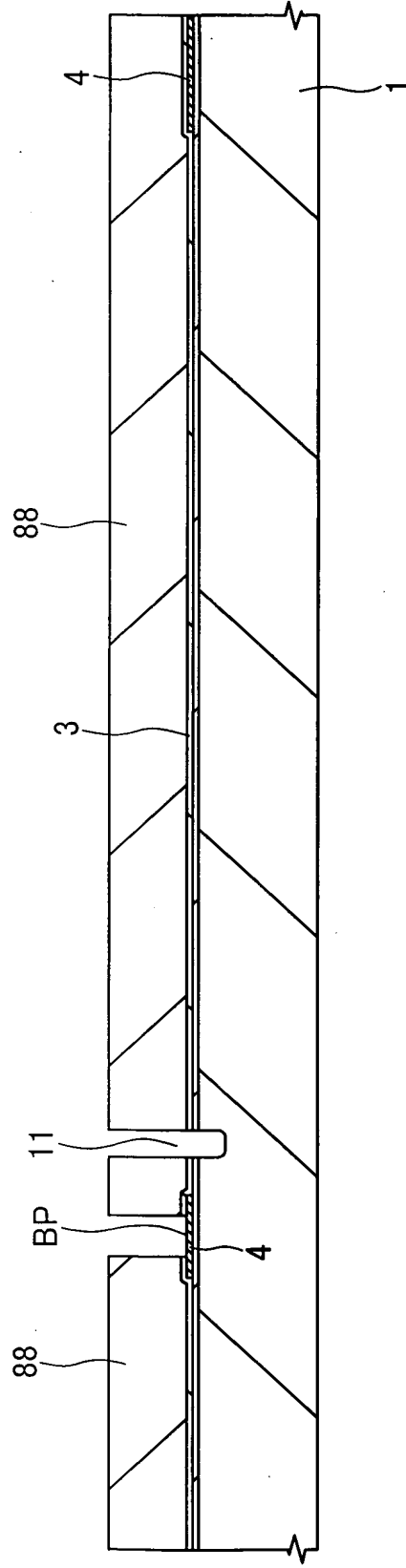
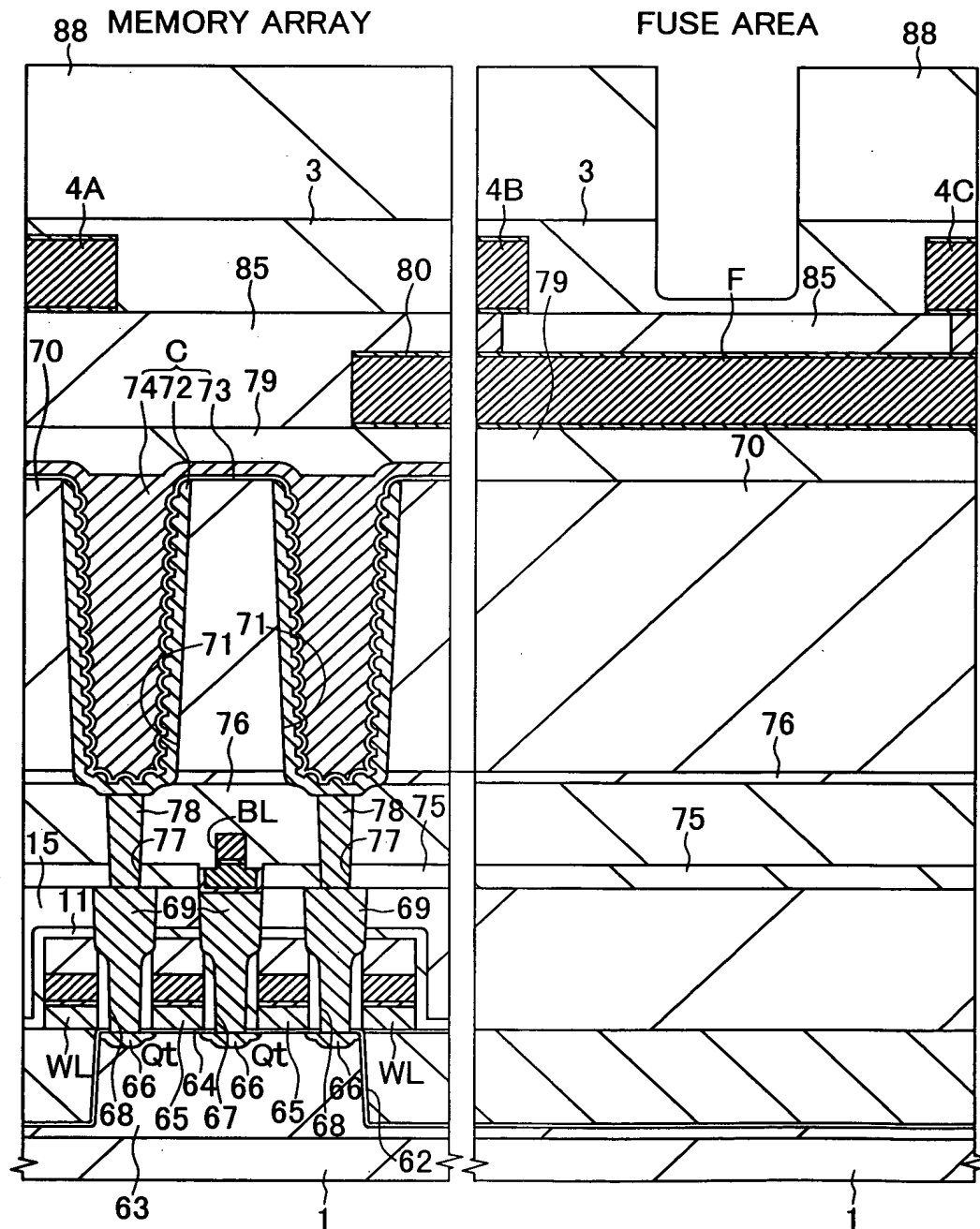


FIG.36



# FIG.37



# FIG.38

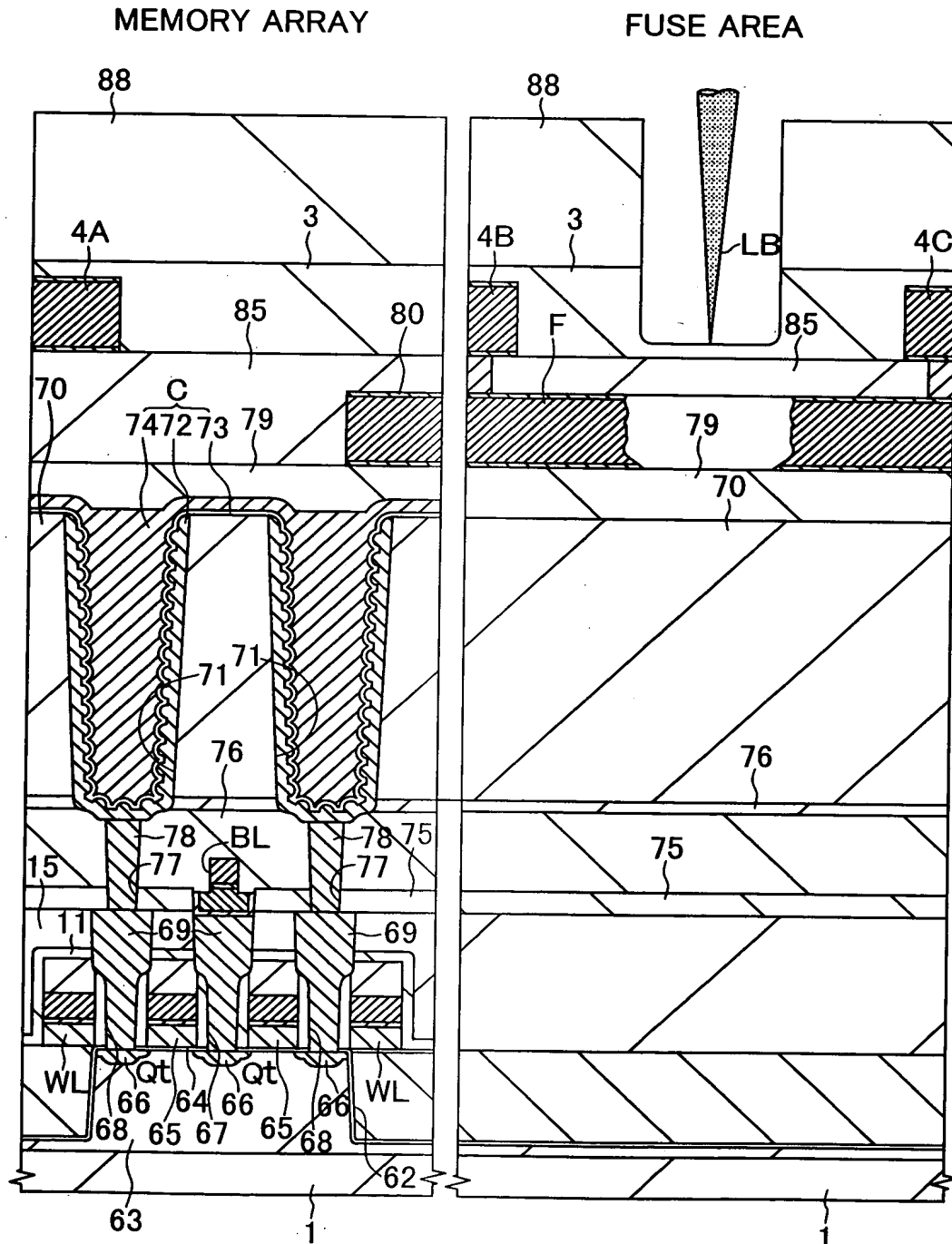


FIG.39

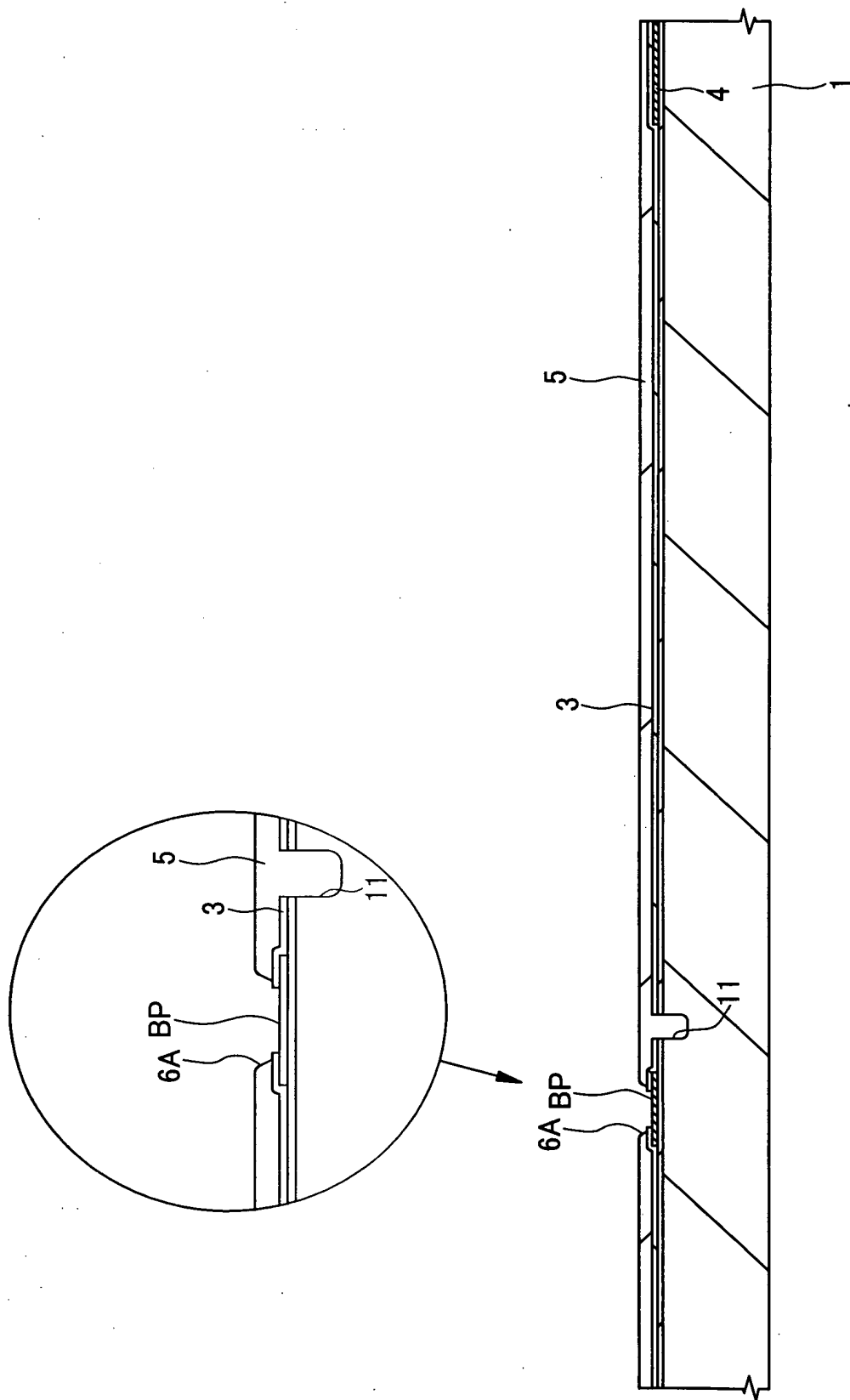


FIG.40

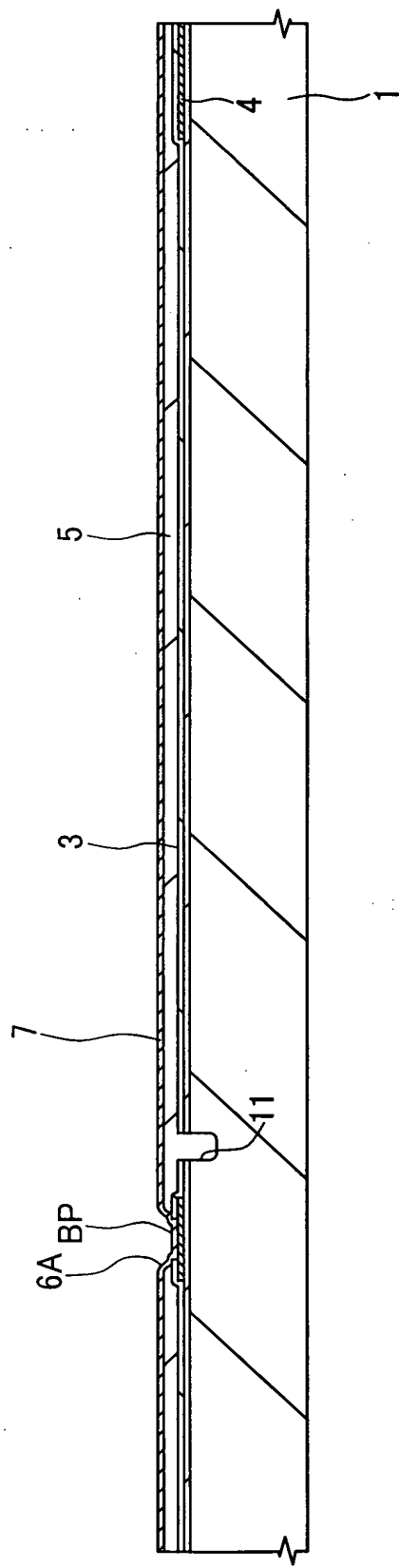




FIG.41

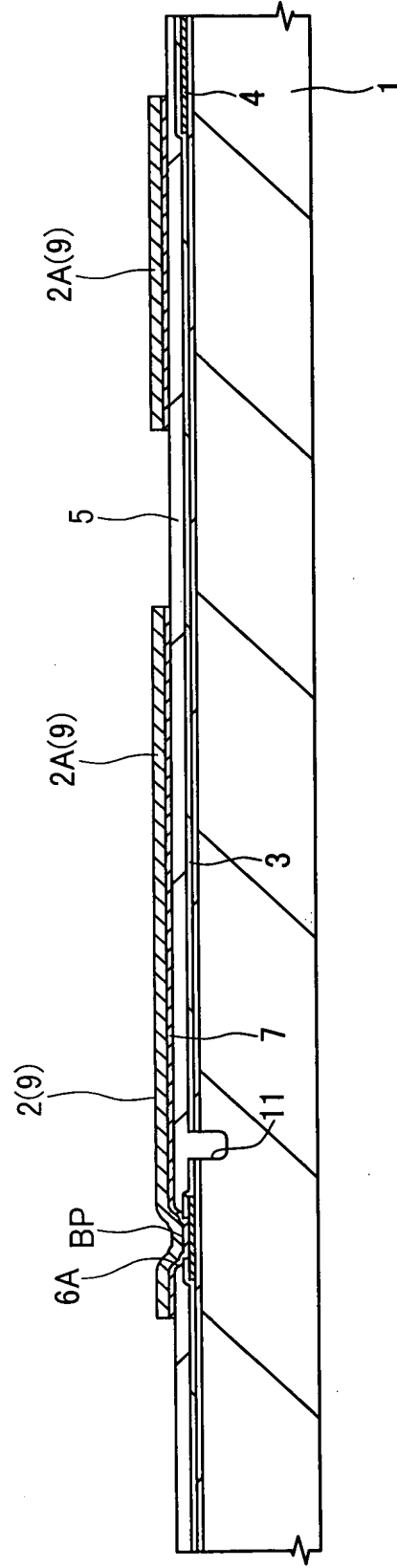


FIG.42

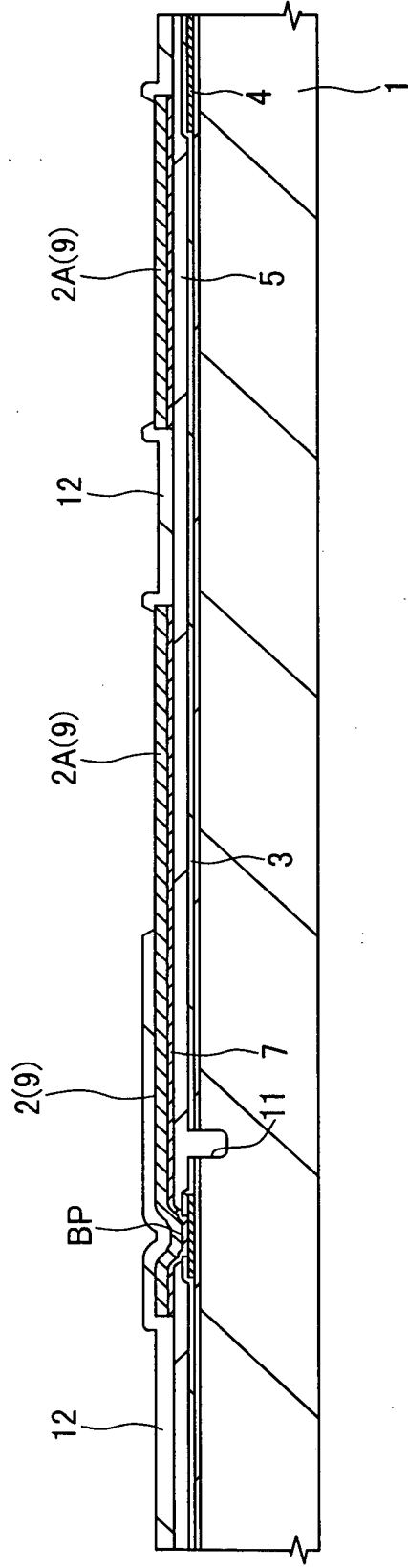


FIG.43

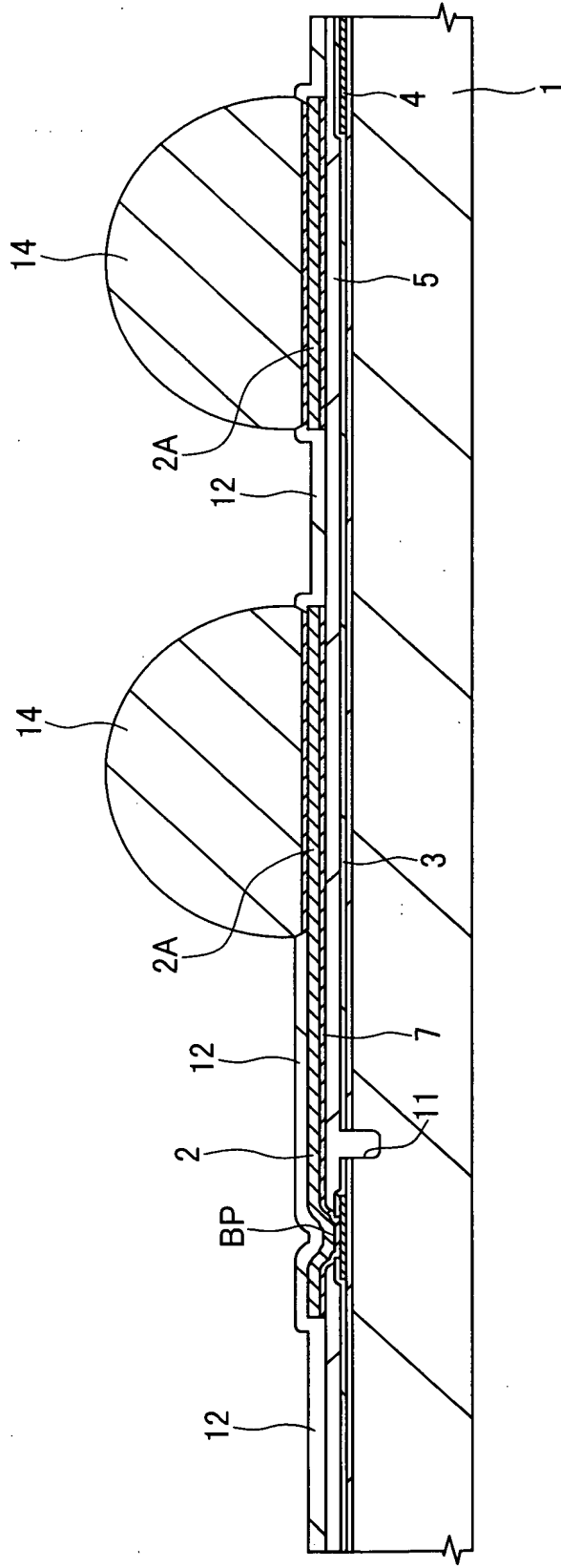


FIG.44

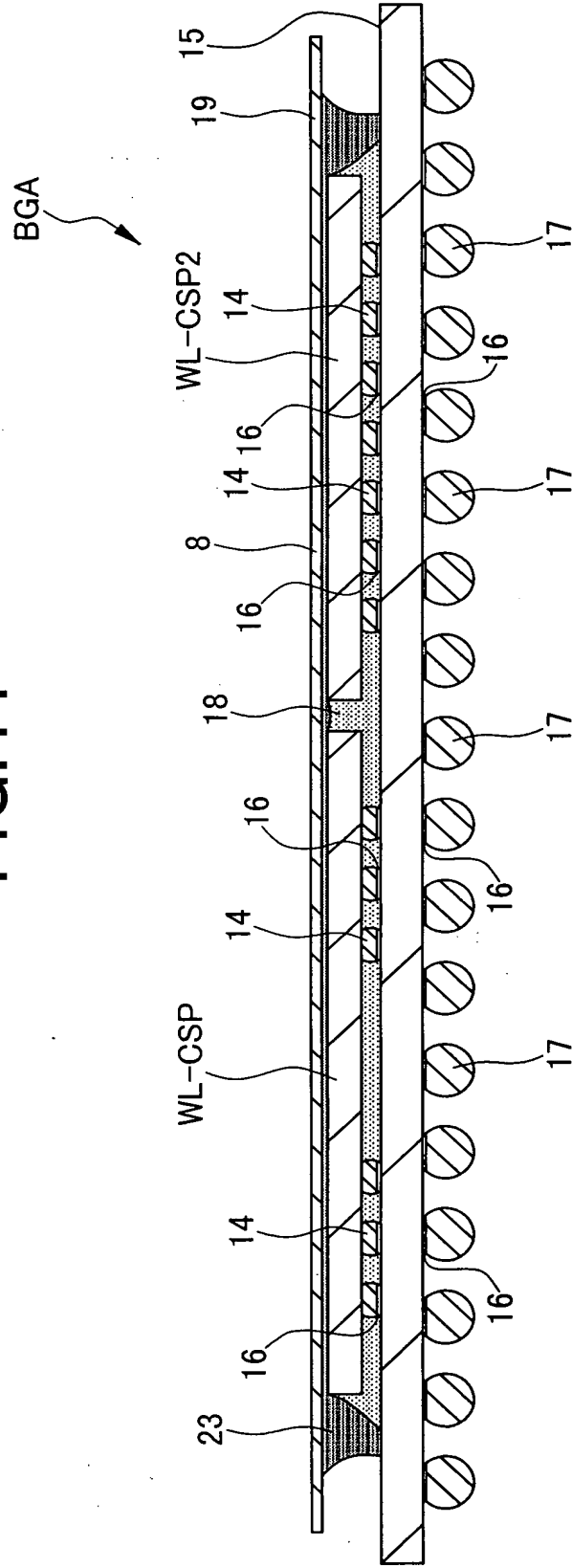


FIG.45

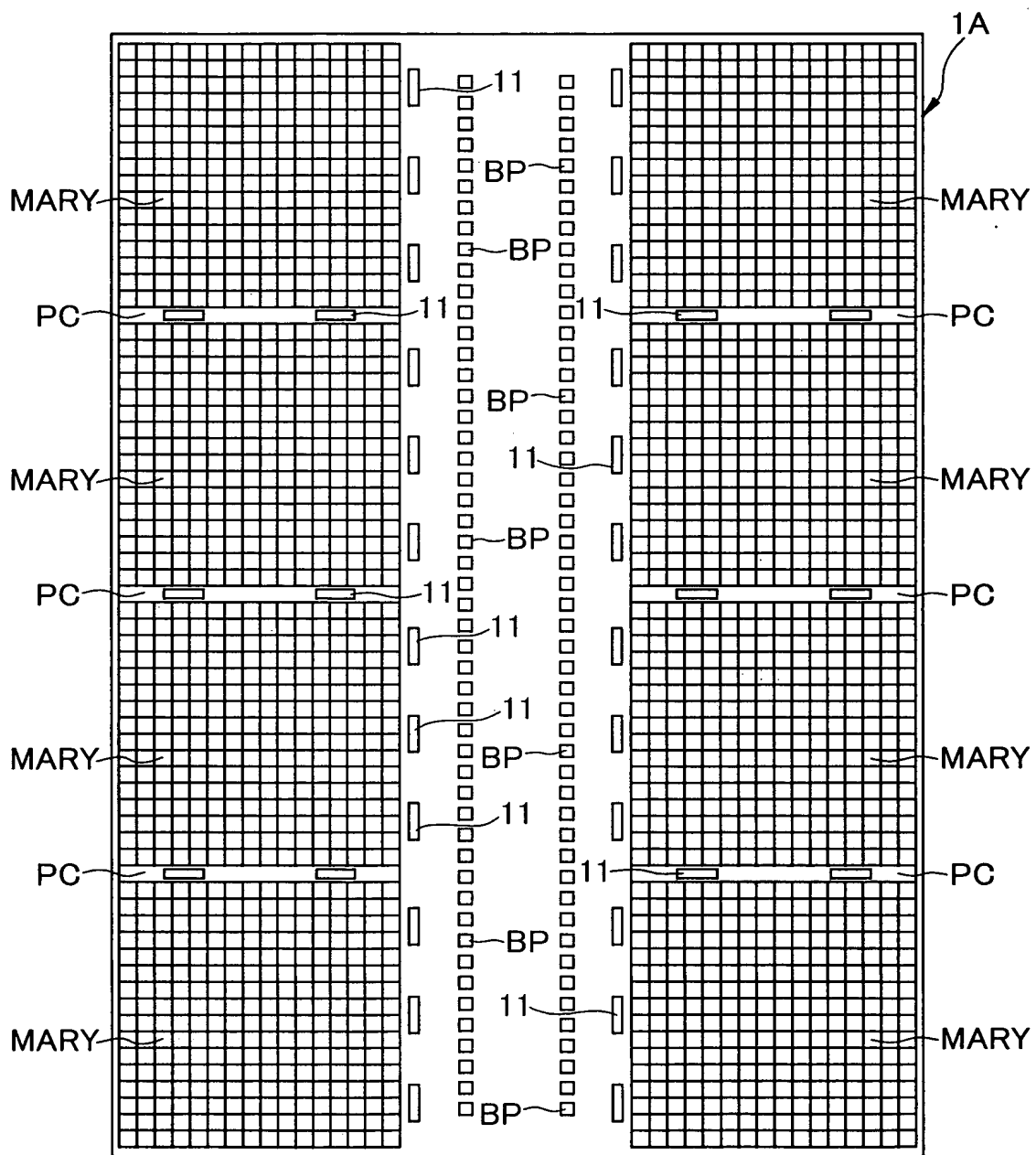


FIG.46

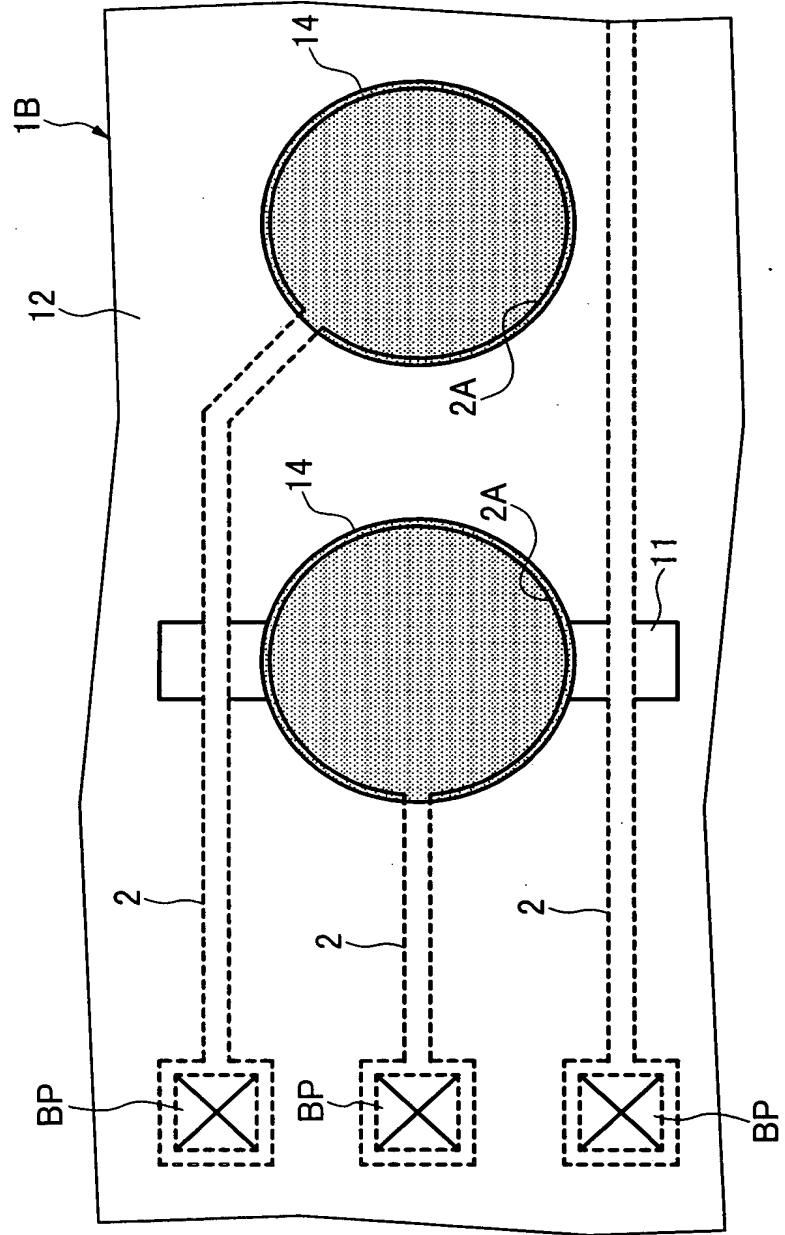


FIG.47

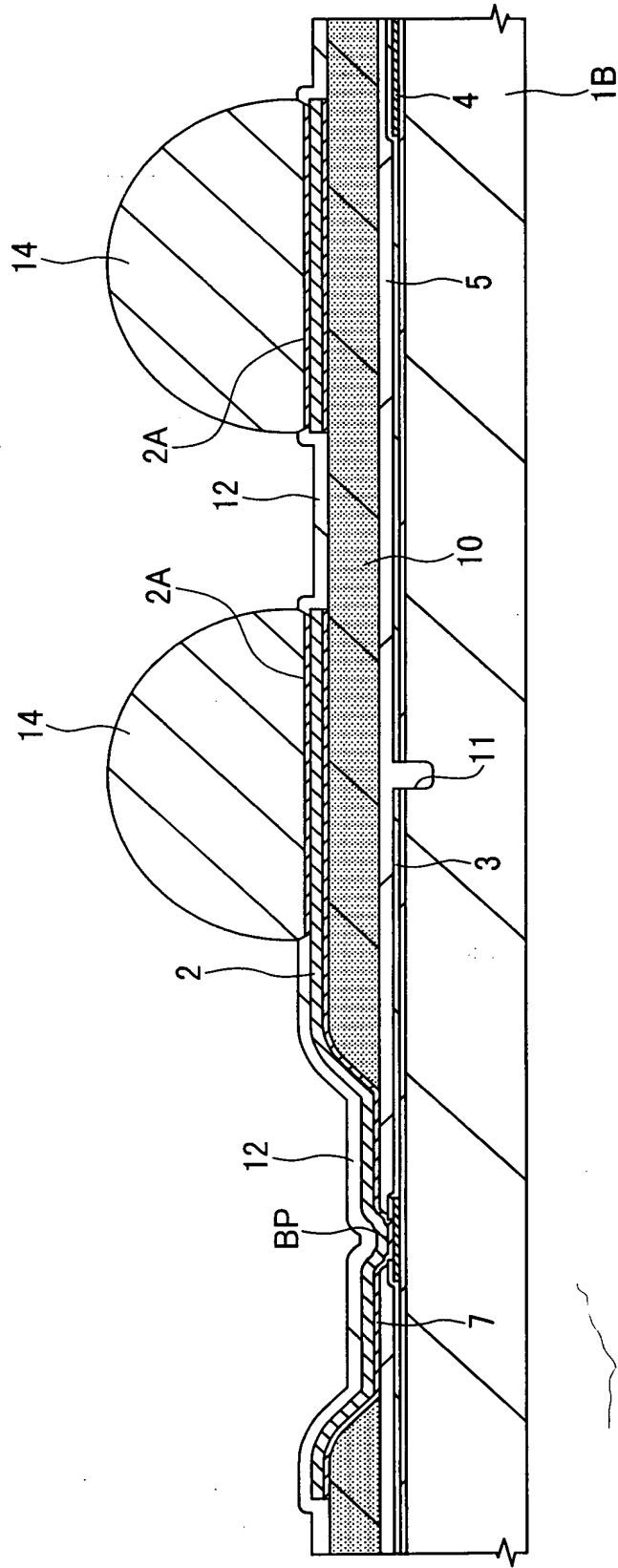
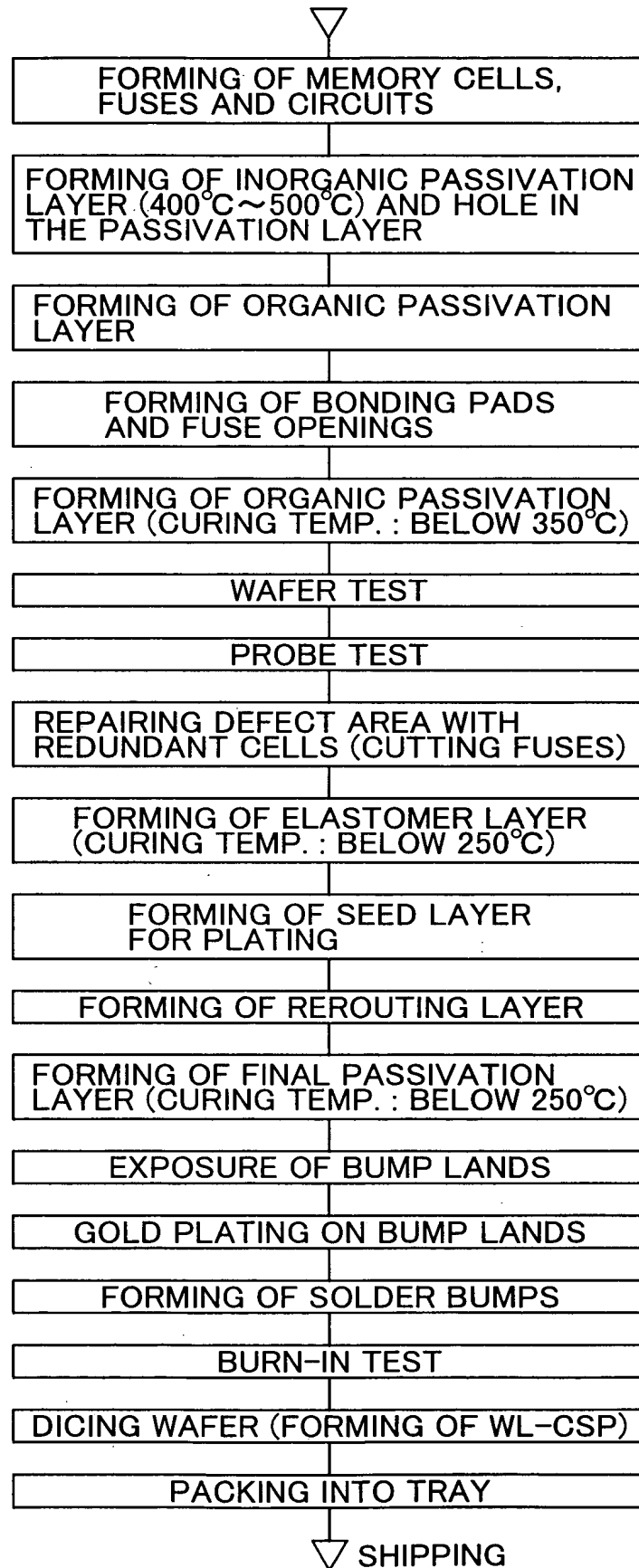


FIG.48





**FIG.49**

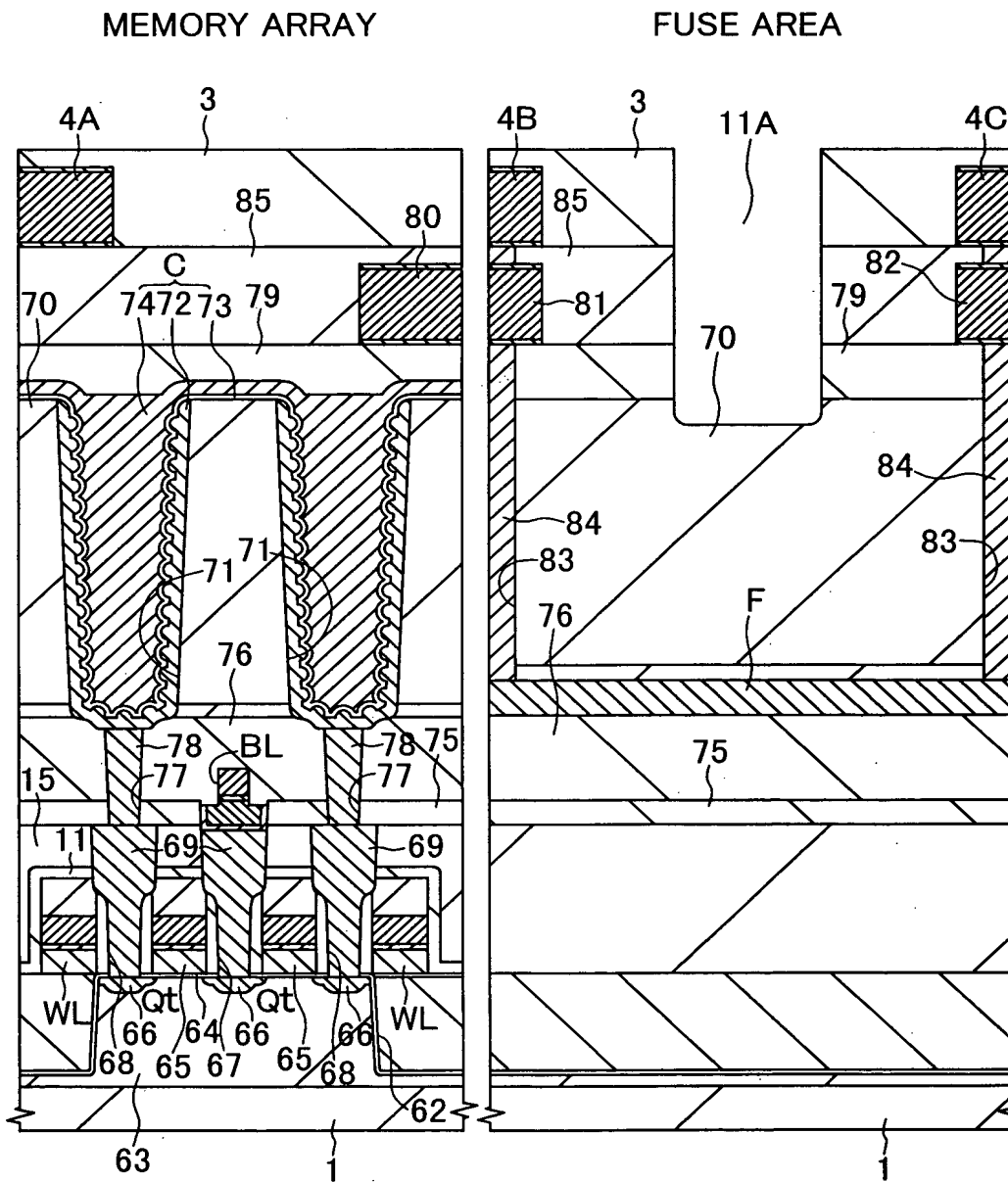
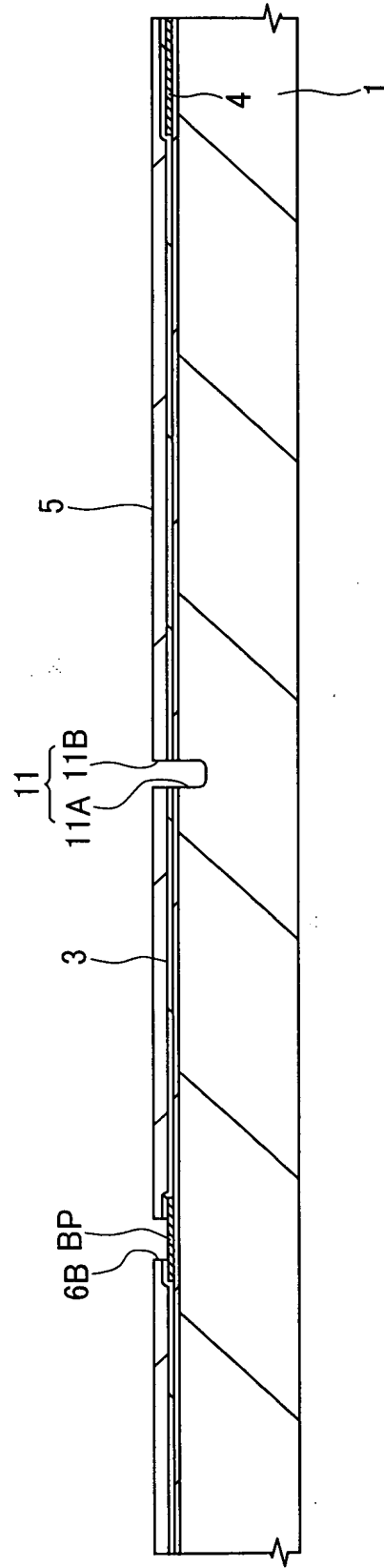


FIG.50



FUSE AREA



FUSE AREA

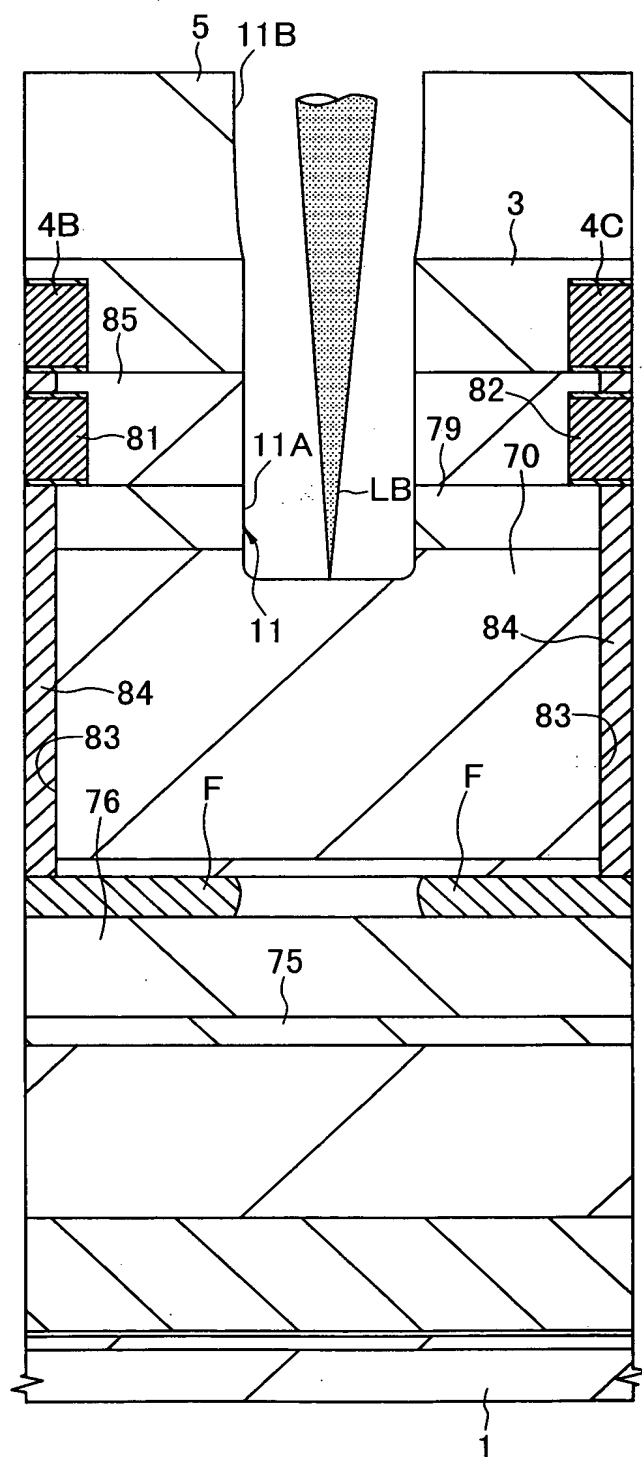


FIG.53

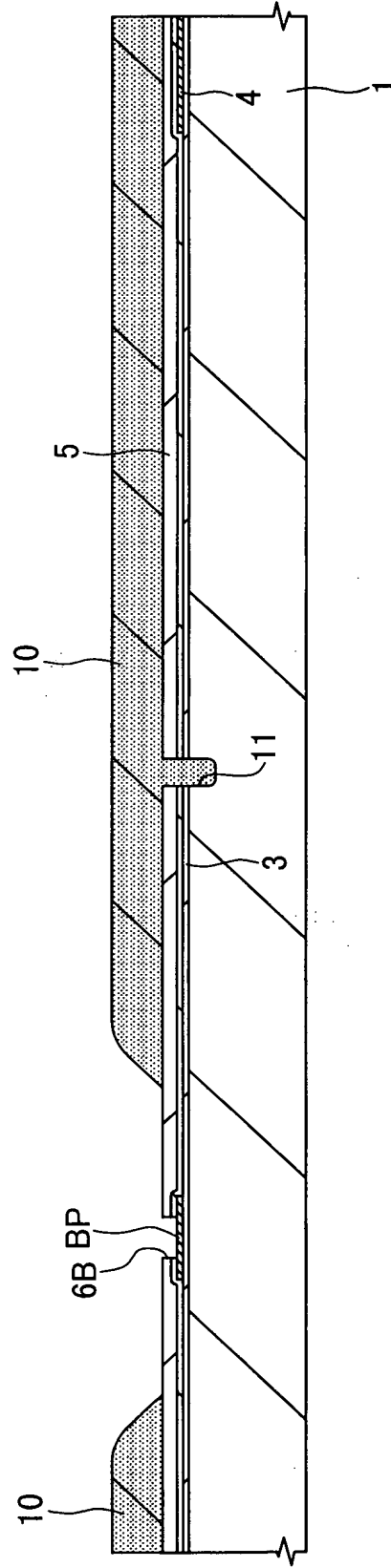


FIG.54

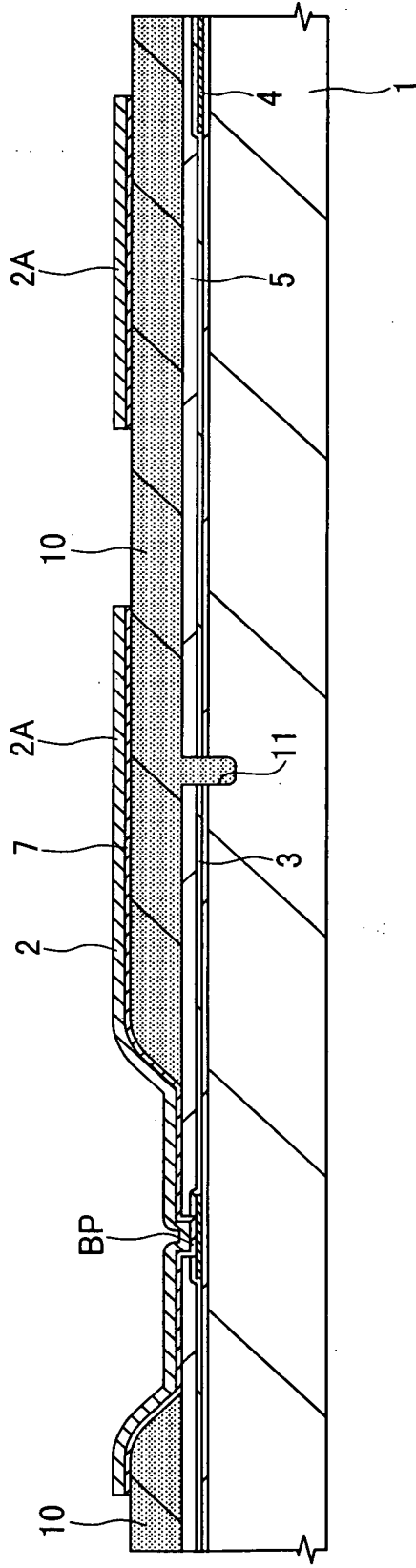


FIG.55

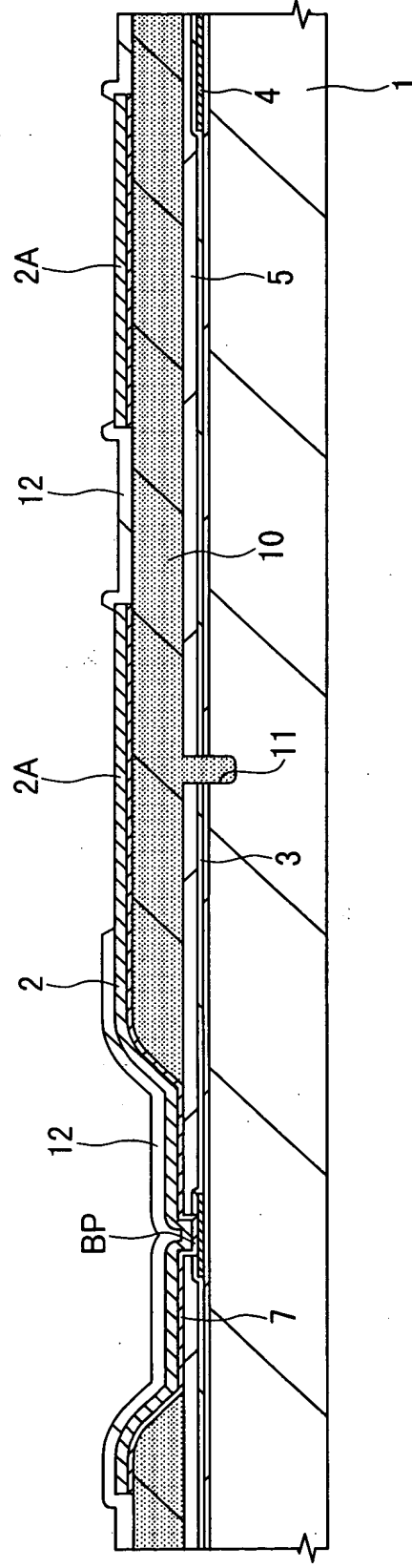


FIG.56

